

Name of Institute: IITE
Name of Faculty: Prof. Ashwin Patani

Course code: EC0319

Course name: Digital Electronics

Pre-requisites: Decimal, Binary Number, Mathematical Analysis, Theorems

Credit points: 4

Offered Semester: 3

Course coordinator (weeks 01 - 12)

Full name: Prof. Ashwin Patani

Department with siting location: Analog Electronics Lab -2nd Floor, Bhanwar Building

Telephone:9824485522

Email: ashwinpatani.ce@indusuni.ac.in

Consultation times:2nd & 4th Saturday

Course lecturer (weeks 01 - 12)

Full name: Prof. Ashwin Patani

Department with siting location Analog Electronics Lab -2nd Floor, Bhanwar Building

Telephone: 9824485522

Email: ashwinpatani.ce@indusuni.ac.in

Consultation times: 2nd & 4th Saturday

Students will be contacted throughout the session via mail with important information relating to this course.

Course Objectives

By participating in and understanding all facets of this course a student will:

- 1) To prepare students to perform the analysis and design of various digital electronic circuits.
- 2) To explain the elements of digital system abstractions such as digital representations of information, digital logic, Boolean algebra, Combinational & Sequential logic, state elements and finite state machine (FSMs).

Course Outcomes (CO)

After successful completion of this course, students will be able to

- 1) To Understand number representation and able to perform conversion between different representation in digital electronic circuits. [BT 2]
- 2) Too Familiar with basic logic gates and Independently or work in team to create logic circuits using logic gates. [BT 6]

- 3) To Remember Boolean algebra and apply basic properties of Boolean algebra to simplify Boolean functions by using the basic Boolean properties. [BT-3]
- 4) To Able to optimize logic circuits using Karnaugh maps. [BT 5]
- 5) To analyze logic processes and implement logical operations using combinational logic circuits. [BT 4]
- 6) To understand concepts of sequential circuits and to analyze sequential systems in terms of state machines. [BT 4]

Course Outline

UNIT-I

[12 hours]

Number System:

Decimal, Binary, Octal, Hexadecimal number system, Conversion of numbers from one number system to other, complement method of addition, subtraction using 9's and 10's complement method & 1's and 2's complement method.

Binary Codes:

Weighted and Non-weighted code, 8421 BCD code, XS-3 code, Grey code, Binary to Grey conversion, Grey to Binary conversion

Logic Gates & Boolean Algebra: AND, OR, NOT, NAND, NOR, X-OR, X-NOR, BUFFER, Axioms and laws of Boolean algebra, D'morgans theorem, Duality, Reduction of Boolean expression.

UNIT-II

[12 hours]

Boolean Algebra - II & Simplification of Boolean Functions: Converting AND/OR/INVERT logic to NAND/NOR logic, POS and SOP expressions, Simplification of Boolean expression using Karnaugh Map for 2 to 5 variables, Don't care conditions and Tabulation method

Combinational Logic: Introduction, Design Procedure, Code Conversion, Multilevel NAND and NOR circuit

UNIT-III

[12hours]

Combinational Circuits with MSI & LSI

The Half-adder, The Full-adder, The Half-subtractor, The Full-Subtractor, Parallel Binary Adders, Binary Subtractor, Adder- Subtractor, BCD adder, Code converters, Parity bit

Generators/Checkers, Comparators, Decoders, BCD to 7-Segment Decoders, Encoders, , Multiplexers, Applications of Multiplexer, De-multiplexers, Circuit implementation using PLDs (PLA, PAL)

Flip Flop:

S-R Flip-flop, JK Flip-flop, D Flip-flop, T Flip-flop, Master-slave Flip-flop, Conversion of Flip flop

UNIT-IV

[12hours]

Shift Registers, Counters & FSM Design

Shift Registers: Serial-in Serial-out Shift register, Serial-in Parallel-out Shift register, Parallel-in Serial-out Shift register, Parallel-in Parallel-out Shift register

Counters: Asynchronous counter, Design of Asynchronous counter, Synchronous counters, Design of Synchronous counter

FSM Design: State Diagram, State Table, State Assignment, Moore and Mealy Model

Method of delivery

(Online Platform ,Face to face lectures, PPT, **Chalkboard**)

Study time

(9 hours per week including class attendance)

CO-PO Mapping (PO: Program Outcomes)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C0 1	3	3	2	1	-	-	-	-	-	-	-	-
C0 2	2	3	3	1	-	-	-	-	2	-	-	-
C0 3	1	3	2	3	-	-	-	-	-	-	-	-
C0 4	2	3	3	2	-	-	-	-	-	-	-	-
C0 5	2	2	3	2	2	-	-	-	-	-	-	-
C0 6	1	2	3	3	3	-	-	-	-	-	-	-

Blooms Taxonomy and Knowledge retention (For reference)

(Blooms taxonomy has been given for reference)

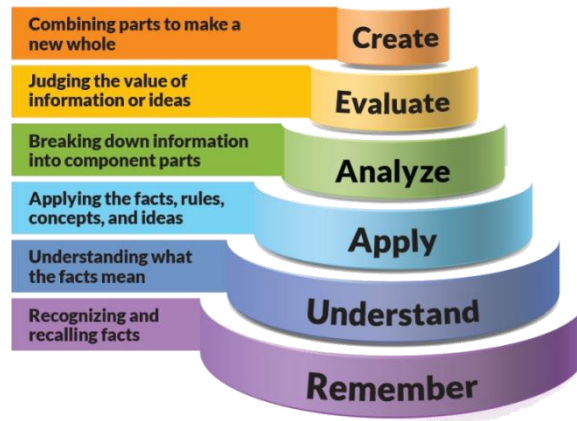


Figure 1: Blooms Taxonomy

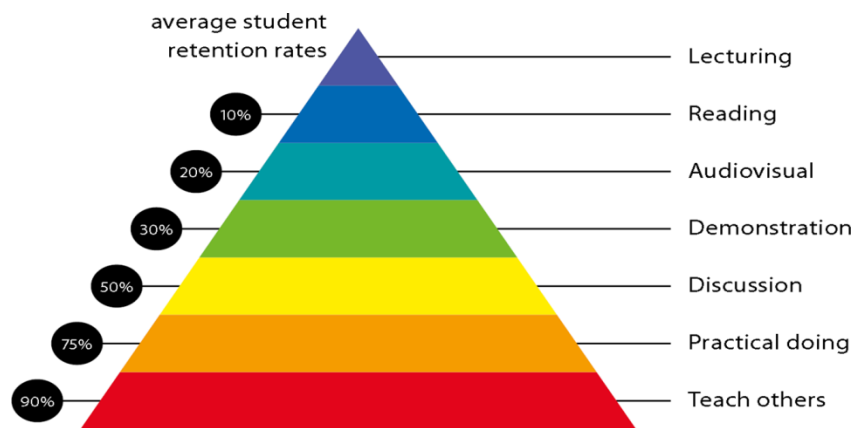


Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered
 (Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of _____ Graduate Capabilities
<p>Informed Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas.</p>	<p>1 Professional knowledge, grounding & awareness</p>
<p>Independent learners Engage with new ideas and ways of thinking and critically analyze issues. Seek to extend knowledge through ongoing research, enquiry and reflection. Find and evaluate information, using a variety of sources and technologies. Acknowledge the work and ideas of</p>	<p>2 Information literacy, gathering & processing</p>

others.	
Problem solvers Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards.	4 Problem solving skills
Effective communicators Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in different settings. Recognize how culture can shape communication.	5 Written communication
	6 Oral communication
	7 Teamwork
Responsible Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.	10 Sustainability, societal & environmental impact

Practical work:

Lab Experiments & Outcome of Digital Logic Design Lab:

Outcome:

Upon successful completion of this course students should be able to:

1. Implementation for basic logic gates & digital Circuits using ICs.
2. Implementation & Analyze the operation of medium & high complexity standard combinational circuits like the encoder, decoder, multiplexer, de-multiplexer, adder, subtractor
3. Implementation & Analyze the operation of a flip-flop and examine relevant timing diagrams
4. Implementation & Analyze the operation of counters and shift registers
5. Design and operate practical digital logic circuits
6. Report findings and evaluate results.

List of Lab Experiment:

1. To Verify the Behavior of Logic Gates using Truth Table and Familiarization with Digital Integrated Circuits
2. Familiarization with the Different Portions of the Datasheet for a Digital IC and Using the Datasheet to Gather Relevant Information to Utilize the IC as a Component in another Digital Logic Circuit
3. Realization of basic gates using Universal Gates.
4. Verification of De-Morgan's Theorem.
5. Implementation of Half Adder & Full Adder Circuits.
6. Implementation of Half Subtractor & Full Subtractor Circuits
7. Implementation of Code Converters using Basic Gates
8. Implementation of Multiplexes (4-1 MUX/8-1 MUX)
9. Implementation of Decoders (3-8 Decoder/4-16 decoder)
10. Realization of Flip-Flop using Gates.
11. Implementation of Shift Registers using Flip Flop. (Serial-in Serial-out Shift register, Serial-in Parallel-out Shift register, Parallel-in Serial-out Shift register, Parallel-in Parallel-out Shift register)
12. Implementation of Asynchronous Counters (4 bit Up/down)
13. Implementation of Synchronous Counters (4 bit Up/down)

Lecture/tutorial times

(Give lecture times in the format below)

Monday: 11.10 – 12.10

Tuesday: 10.00 – 11.00 am

Wednesday: 11.10 – 12.10 am

Lab: Friday: 9:00-11:00 am

Attendance Requirements

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for semester examinations.

Details of referencing system to be used in written work

Text Books:

- 1) Morris Mano, "Digital Logic and Computer Design", Pearson , ISBN 13: 9788177584097

Reference Books:

- 1) Ronald J. Tocci, Gregory L. Moss, "Digital Systems", 10 Ed, Pearson, ISBN 9780135103821
- 2) D.C.Green, "Digital Electronics"5th Ed., Pearson, 2005, ISBN-9788177580686

Web Resources:

- 1) Digital Circuits & Systems (<http://nptel.ac.in/courses/117106086/1>)
- 2) Circuits and Electronics (<https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-002-circuits-and-electronics-spring-2007/index.htm>)

ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:

CIE 60 marks:
(40 marks mid semester examination + 20 marks internal evaluation)

Internal Evaluation (20 Marks):
05 marks: attendance
10 marks: Seminar Presentation
05 marks: Assignment

Final exam (closed book) 40 Marks

SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in internal component or less than 40% in the end semester will be considered for supplementary assessment in the respective components (i.e internal component or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (internal component or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of -% of the maximum mark per calendar day

Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

Retention of Written Work

Written assessment work will be retained by the Course coordinator/lecturer for two weeks after marking to be collected by the students.

University and Faculty Policies

Students should make themselves aware of the University and/or Faculty Policies regarding plagiarism, special consideration, supplementary examinations and other educational issues and student matters.

Plagiarism - Plagiarism is not acceptable and may result in the imposition of severe penalties. Plagiarism is the use of another person's work, or idea, as if it is his or her own - if you have any doubts at all on what constitutes plagiarism, please consult your Course coordinator or lecturer. Plagiarism will be penalized severely.

Do not copy the work of other students.

Do not share your work with other students (except where required for a group activity or assessment)

Course schedule (subject to change)

(Mention quiz, assignment submission, breaks etc as well in the table under the Teaching Learning Activity Column)

Week #	Topic & contents	CO Addressed	Teaching Learning Activity (TLA)
Weeks 1	Number System: Decimal, Binary, Octal, Hexadecimal number system, Conversion of numbers from one number system to oth	1	White Board,PPT
Weeks 2	complement method of addition ,subtraction using 9's and 10's compliment method & 1's and 2's complement method	1	White Board,PPT
Week 3	Binary Codes: Weighted and Non-weighted code, 8421 BCD code, XS-3 code, Gray code, Binary to Gray conversion, Gray to Binary conversion	1	White Board,PPT
Week 4	Logic Gates & Boolean Algebra: AND, OR, NOT, NAND, NOR, X-OR, X-NOR, BUFFER, Axioms and laws of Boolean algebra, D'morgans theorem, Duality, Reduction of Boolean expression.	2,3	White Board,PPT Assignment Submission
Week 5	Boolean Algebra - II & Simplification of Boolean Functions: Converting AND/OR/INVERT logic to NAND/NOR logic , POS and SOP expressions	1,2,3	White Board,PPT
Week 6	Simplification of Boolean expression using Karnaugh Map for 2 to 5 variables, Don't care conditions and Tabulation method	3,4	BB,PPT Mid Semester Examination
Week 7	Combinational Logic: Introduction, Design Procedure, Code Conversion, Multilevel NAND and NOR circuit	3,5	White Board,PPT

Week 8	Combinational Circuits with MSI & LSI The Half-adder, The Full-adder, The Half-subtractor, The Full-Subtractor, Parallel Binary Adders, Binary Subtractor, Adder- Subtractor, BCD adder, Code converters, Parity bit Generators/Checkers	3,5	White Board,PPT
Week 9	Comparators, Decoders, BCD to 7-Segment Decoders, Encoders, , Multiplexers, Applications of Multiplexer, Demultiplexers , Circuit implementation using PLDs (PLA, PAL)	3,5	White Board,PPT
Week 10	Flip Flop : S-R Flip-flop, JK Flip-flop, D Flip-flop, T Flip-flop, Master-slave Flip-flop,	3,4	White Board,PPT
Week 11	Conversion of Flip flop	3,6	White Board,PPT
Week 12	Shift Registers: Serial-in Serial-out Shift register, Serial-in Parallel-out Shift register, Parallel-in Serial-out Shift register, Parallel-in Parallel-out Shift register	3,6	White Board,PPT
Week 13	Counters: Asynchronous counter, Design of Asynchronous counter,	3,6	White Board,PPT Seminar Presentation
Week 14	Synchronous counters, Design of Synchronous counter	3,6	White Board,PPT Seminar Presentation
Week 15	FSM Design: State Diagram, State Table, State Assignment, Moore and Mealy Model	3,6	White Board,PPT Seminar Presentation

PROGRAM MAP:

