### Name of Institute: Indus Institute of Technology and Engineering.

### Name of Faculty: Prof. Miloni Ganatra

**Course code: EC0616**

**Course name: VLSI Design**

Pre-requisites: Digital Logic Design (EC0301)

Credit points: 5

Offered Semester: 6th

**Course Coordinator (weeks 01 - 12)**

Full Name: Miloni Ganatra

Department with sitting location: 2nd Floor, EEE lab 2 , Bhanwar Building

Telephone: 9974592124

Email: miloniganatra.ee@indusuni.ac.in

Consultation times: Monday,Tuesday 3:45 to 4:15pm ,All working Saturdays

**Course Lecturer (weeks 01 - 12)**

Full Name: Miloni Ganatra

Department with sitting location: 2nd Floor, EEE lab 2 , Bhanwar Building

Telephone: 9974592124

Email: miloniganatra.ee@indusuni.ac.in

Consultation times: Monday,Tuesday 3:45 to 4:15pm ,All working Saturdays

Students will be contacted throughout the Session via Mail with important information relating to this Course.

# Course Objectives

1. The main objective of the course is to bring out circuit and system level views on VLSI design on the same platform.
2. In this course, student will learn the basic device (MOSFET) used to implement the VLSI design and then deals with complex digital circuits keeping in mind the current trend in technology.
3. After completion of the course, student will be able to understand design perspective, from basic specifications to system level blocks.

# Course Outcomes (CO)

By participating in and understanding all facets of this Course a student will be able to:

1. Calculate the R-C delay of different gate using Elmore’s delay method.
2. Analyze and optimize the delay of the critical data path using logical effort technique.
3. Design complex logic gates using different logic styles like CMOS, Pass Transistor Logic, and Transmission Gate etc.
4. Design and implement the Combinational circuits and sequential circuits at transistor level.
5. Test the different design for stuck at faults. and learn the different methods for testing.
6. Learn the different methods for testing at circuit level.

# Course Outline

**UNIT-I**

**Introduction to VLSI**

Introduction, NMOS/PMOS manufacturing, CMOS process steps, Physics of MOS, characteristics of the MOSFET, Threshold voltage, gradual channel approximation, channel length modulation, Scaling of MOSFET, Short channel effects, Narrow channel effects, Latch-up and its prevention in CMOS, SPICE model of MOSFET, Physical design of MOSFET in CAD

**UNIT-II**

**MOS Inverters: Dynamic and Static characteristics**

Resistive load inverters, CMOS inverters, Analysis, design, Power consumptions in inverters, Interconnects and parasitic assisted handoff and soft handoff, Introduction to dropped call rate, Formula of dropped call rate

**UNIT-III**

**MOS Logic Circuits**

Introduction, Combinational MOS Logic Circuits, Sequential MOS Logic circuits, Dynamic Logic Circuits, CMOS Transmission Gates, Schmitt trigger circuits, Voltage Bootstrapping, Pass transistor circuits, High performance CMOS dynamic circuits, Low-power CMOS Logic circuits.

**UNIT-IV**

**Sequential MOS Logic Circuits:**

Introduction, Behavior of Bi-stable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop

**Design for testability:**

Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques

# Method of delivery

Lectures, Power Point Slides, Tutorial, Quiz, Test, and Understanding of design techniques using simulations.

# Study time

7 hours per week.

# CO-PO Mapping (PO: Program Outcomes)

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **PO****1** | **PO****2** | **PO****3** | **PO****4** | **PO****5** | **PO****6** | **PO****7** | **PO****8** | **PO****9** | **PO****10** | **PO****11** | **PO****12** |
| **CO1** | 2 | 3 | 1 | 2 | 2 | - | - | - | - | - | - | - |
| **CO2** | 3 | 3 | 2 | 3 | 3 | - | - | - | - | - | - | - |
| **CO3** | 2 | 2 | 3 | - | 2 | - | - | - | - | - | 2 | - |
| **CO4** | 3 | - | 3 | - | - | - | - | - | - | - | 2 | - |
| **CO5** | 1 | 2 | - | 2 | - | - | - | - | - | - | - | - |
| **CO6** | 2 | 2 | - | 2 | 1 |  |  |  |  |  | - | 2 |

# Blooms Taxonomy and Knowledge retention (For reference)

(Blooms taxonomy has been given for reference)



**Figure 1: Blooms Taxonomy**



**Figure 2: Knowledge retentio**

# Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

|  |  |
| --- | --- |
| **General Graduate Qualities** | **Specific Department of \_\_\_\_\_\_Graduate Capabilities** |
| **Informed**Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas. | **1 Professional knowledge, grounding & awareness** |
| **Independent learners**Engage with new ideas and ways of thinking and critically analyze issues. Seek to extend knowledge through ongoing research, enquiry and reflection. Find and evaluate information, using a variety of sources and technologies. Acknowledge the work and ideas of others. | **2 Information literacy, gathering & processing** |
| **Problem solvers**Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards. | **4 Problem solving skills** |
| **Effective communicators**Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in different settings. Recognize how culture can shape communication. | **5 Written communication** |
| **6 Oral communication** |
| **7 Teamwork** |
| **Responsible**Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.  | **10 Sustainability, societal & environmental impact** |

# Practical work:

Practical work in this course starts with the design of basic gates using different logic families. Student will learn to characterize their design by measuring the four parameters: 1. Power, 2. Area, 3. Delay, and 4. Power Delay Product. At the end of this course student will be able design the system blocks at transistor level.

# Lecture/tutorial times

Lecture Tuesday 11:55 – 12:50 pm

Lecture Tuesday 01:30 – 02:25 pm

Lecture Friday 11:55 – 12:50 pm

Laboratory Friday 09:00-10:50 am

# Attendance Requirements

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the Course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for mid and end semester examinations.

# Details of referencing system to be used in written work

# Text books

# Neil H. E. Weste, David Money Harris “CMOS VLSI Design: A circuit and Systems Perspective” Pearson, 3rd edition.

# [Jan M. Rabaey](http://dl.acm.org/author_page.cfm?id=81100063897&coll=DL&dl=ACM&trk=0&cfid=695307506&cftoken=99026290) “Digital integrated circuits: a design perspective” Prentice-Hall 2nd edition.

# Additional Materials

NPTEL Course: CMOS Digital VLSI Design.

Link: https://onlinecourses.nptel.ac.in/noc19\_ee25/course

# ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:

Theory:

Class Test/Quiz (10 Marks)

Seminar Presentation (10 Marks)

MSE (40 Marks)

ESE (40 Marks)

Practical:

Mini Project (20 Marks)

Practical Performance + Lab manual (40 Marks)

ESE (40 Marks)

# SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in mid semester or end semester will be considered for supplementary assessment in the respective components (i.e mid semester or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (mid semester or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

# Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

# Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of -20% of the maximum mark per calendar day

# Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

# Retention of Written Work

Written assessment work will be retained by the Course coordinator/lecturer for two weeks after marking to be collected by the students.

# University and Faculty Policies

Students should make themselves aware of the University and/or Faculty Policies regarding plagiarism, special consideration, supplementary examinations and other educational issues and student matters.

**Plagi**a**rism** - Plagiarism is not acceptable and may result in the imposition of severe penalties. Plagiarism is the use of another person’s work, or idea, as if it is his or her own - if you have any doubts at all on what constitutes plagiarism, please consult your Course coordinator or lecturer. Plagiarism will be penalized severely.

***Do not copy the work of other students.***

***Do not share your work with other students (except where required for a group activity or assessment).***

# Course schedule (subject to change)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Week #**  | **Topic & contents**  | **CO Addressed** | **Teaching Learning Activity (TLA)** |
|  | Weeks 1 | Introduction, MOSFET I/V Characteristics, Channel length modulation | 1-2 | BB,PPT |
| Weeks 2 | MOSFET C/V Characteristics Second Order Effects | 1-2 | BB,PPT |
| Week 3 | CMOS inverter DC CharacteristicsBeta Ratio EffectsNoise MarginsPass Transistor DC CharacteristicsTristate Inverter Switch level RC delay model | 1-3 | BB,PPT |
| Week 4 | RC Delay ModelLinear Delay ModelLogical Effort | 2-3 | BB,PPT |
| Week 5 | Parasitic DelayDelay in a Logic GateDelay in Multistage Logic NetworksChoosing the Best Number of Stages | 2-4 | BB,PPT |
|  |  |
|  | Week 6 | Limitations of Logical EffortDynamic PowerStatic Power | 3-4 | BB,PPT |
| Week 7 | **Combinational Circuit Design**Pass-Transistor CircuitsStatic CMOS | 4 | BB,PPT |
| Week 8 | Ratioed CircuitsPass-Transistor Circuits | 4 | BB,PPT |
| Week 9 | Sequencing Static CircuitsMax-Delay ConstraintsMin-Delay Constraints | 3-4 | BB,PPT |
|  | Week 10 | Time BorrowingClock SkewCircuit Design of Latches and Flipflops | 4 | BB,PPT |
| Week 11 | Fault ModelsDesign for Testability | 5 | BB,PPT |
|  | Week 12 | Ad-hoc testingScan chain based testingBISTIDDQ testing | 5 | BB,PPTl |

**Program map for B.Tech (Electronics & Communication Engineering)**

