ज्ञानेन प्रकाशते जगत्
INDUS UNIVERSITY

MICROPROCESSORS

(Subject Code-CE0506/CS0506)

Unit-3

B.Tech (CE/CSE)

Semester-V

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Peripheral IC Interfacing

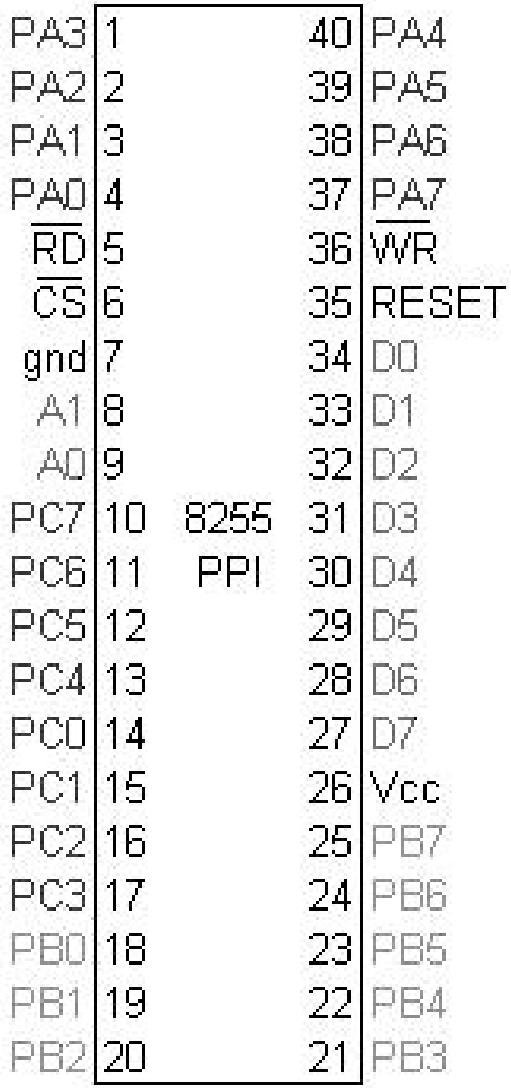
8255

8255 Programmable Peripheral Interface

- The 8255 is a widely used, programmable parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. (40 pin IC)

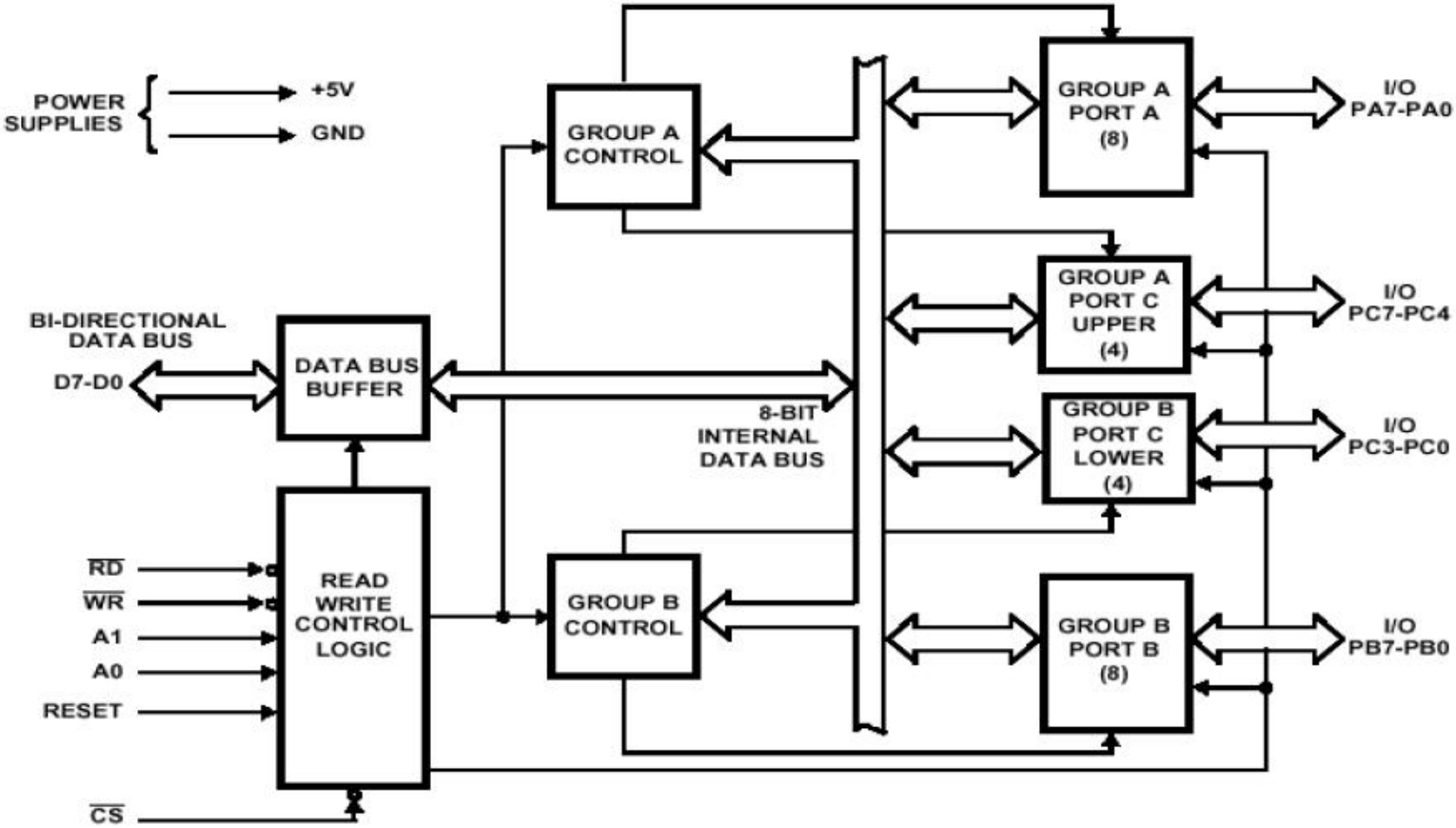
- The 8255 has 24 I/O pins that can be grouped primarily into two 8 bit parallel ports: A and B, with the remaining 8 bits as Port C. The 8 bits of port C can be used as individual bits or be grouped into two 4 bit ports : CUpper (CU) and CLower (CL). The functions of these ports are defined by writing a control word in the control register.

8255 Pin Diagram



- 8255 can be used in two modes: Bit set/Reset (BSR) mode and I/O mode.
- The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into 3 modes: mode 0, mode 1 and mode 2. In mode 0, all ports function as simple I/O ports.
- Mode 1 is a handshake mode whereby Port A and/or Port B use bits from Port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status check and interrupt.
- In mode 2, Port A can be set up for bidirectional data transfer using handshake signals from Port C, and Port B can be set up either in mode 0 or mode 1.

Block Diagram



Control Pins

$\overline{RD}$ (Read) : This signal enables the Read operation. When the signal is low, microprocessor reads data from a selected I/O port of 8255.

$\overline{WR}$ (Write) : This control signal enables the write operation.

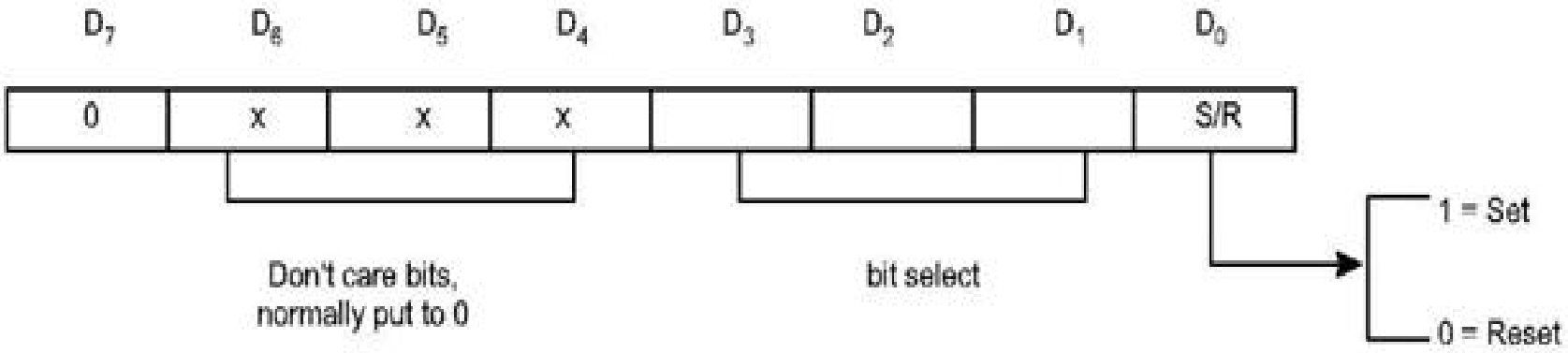
RESET (Reset) : It clears the control registers and sets all ports in input mode.

$\overline{CS}$, A0, A1 : These are device select signals. is connected to a decoded address and A0, A1 are connected to A0, A1 of microprocessor.

Port Selection

$\overline{CS}$	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	x	x	8255 is not selected

BSR Mode of 8255



D_3	D_2	D_1	*Particular bit of Port C selected*
0	0	0	Bit 0
0	0	1	Bit 1
0	1	0	Bit 2
0	1	1	Bit 3
1	0	0	Bit 4
1	0	1	Bit 5
1	1	0	Bit 6
1	1	1	Bit 7

Write a program to perform the following operations.

(1) reset bit 7 of port c

(2) set bit 5 of port c

Assume the address of Port A = 80H, B = 82H, C = 84H, CWR = 86H.

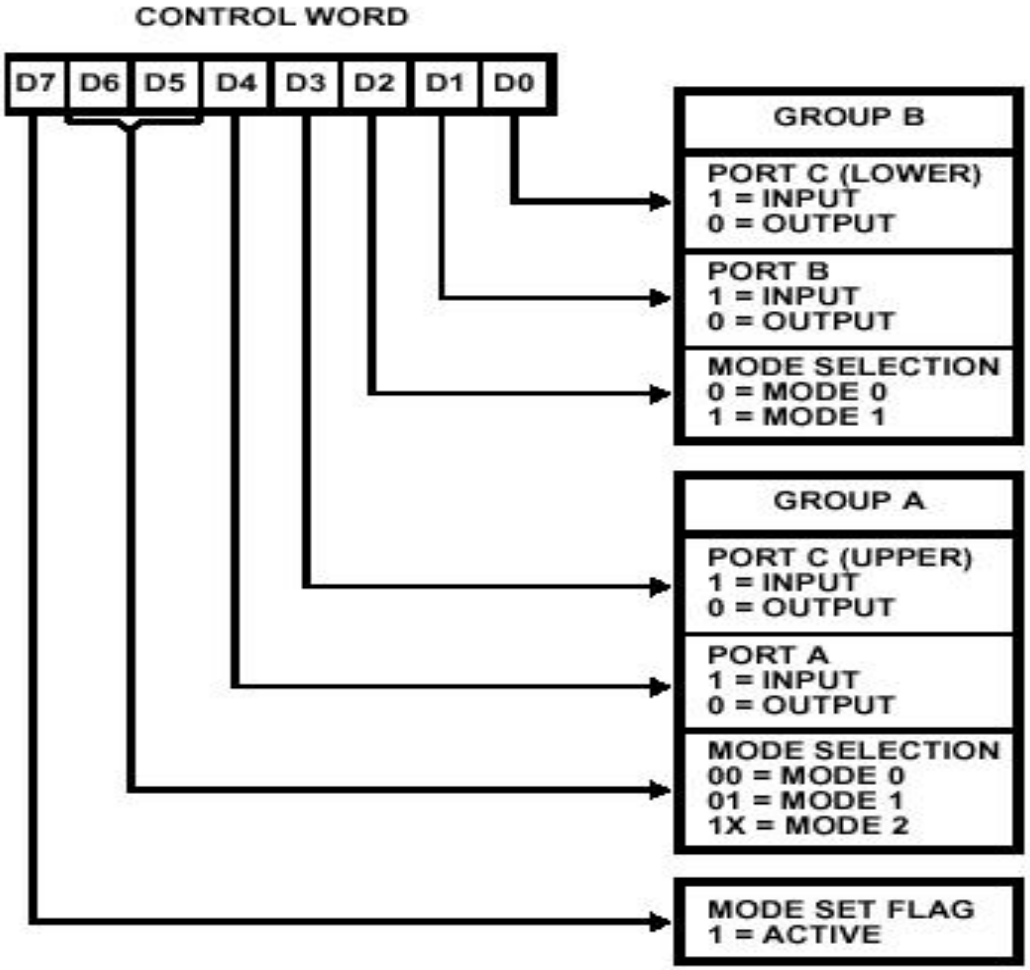
(1) To reset the bit 7 of port c

```
MOV  AL, 7EH
MOV 86H,AL
```

(2) To set bit 5 of port C

```
MOV AL,7BH
MOV 86H,AL
```

Control Word Format



Programming 8255

- Mode 0:

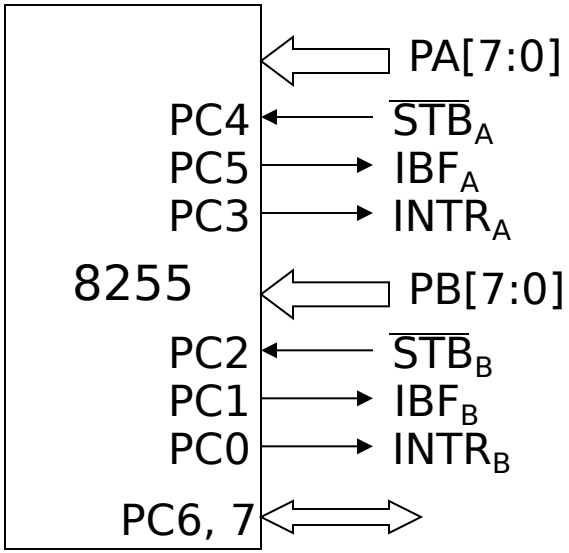
— Ports A, B, and C can be individually programmed as input or output ports
— Port C is divided into two 4-bit ports which are independent from each oth

Write a program to Read the switches connected to PORT B and display the values on LED's Connected to PORT A. Assume the address of Port A = 80H, B = 82H, C = 84H, CWR = 86H.

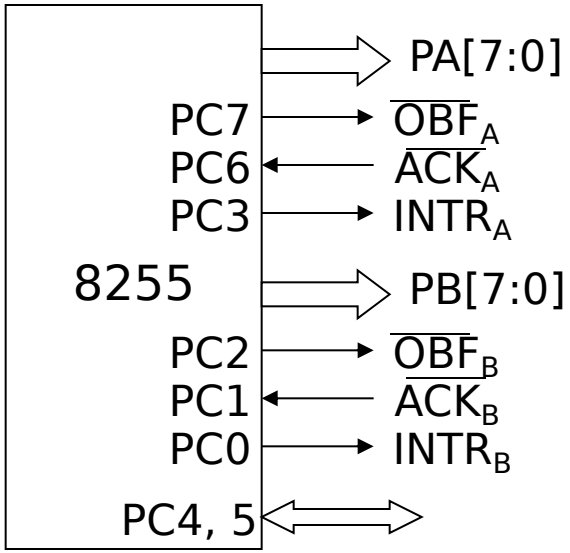
```
MOV AL,8AH
OUT 86H,AL
RPT:  IN AL, 82H
OUT 80H,AL
JMP RPT
```

- Mode 1:
  - — Ports A and B are programmed as input or output ports
  - — Port C is used for handshaking / Strobe

Input



Output



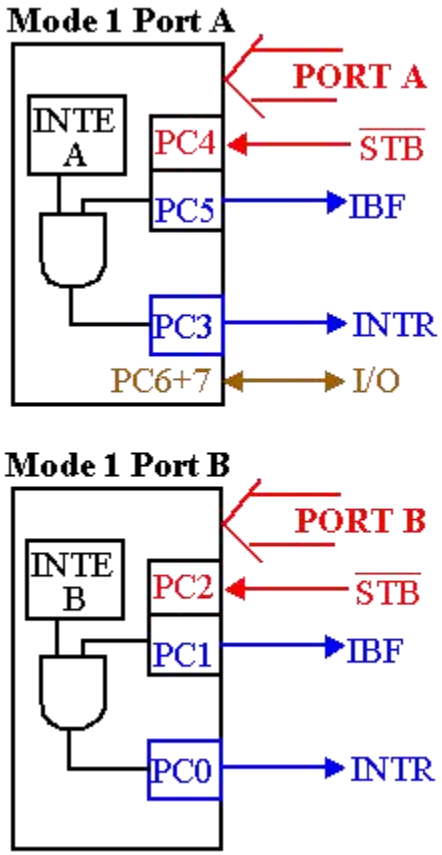
$\overline{\text{STB}}$ The strobe input loads data into the port latch on a 0-to-1 transition

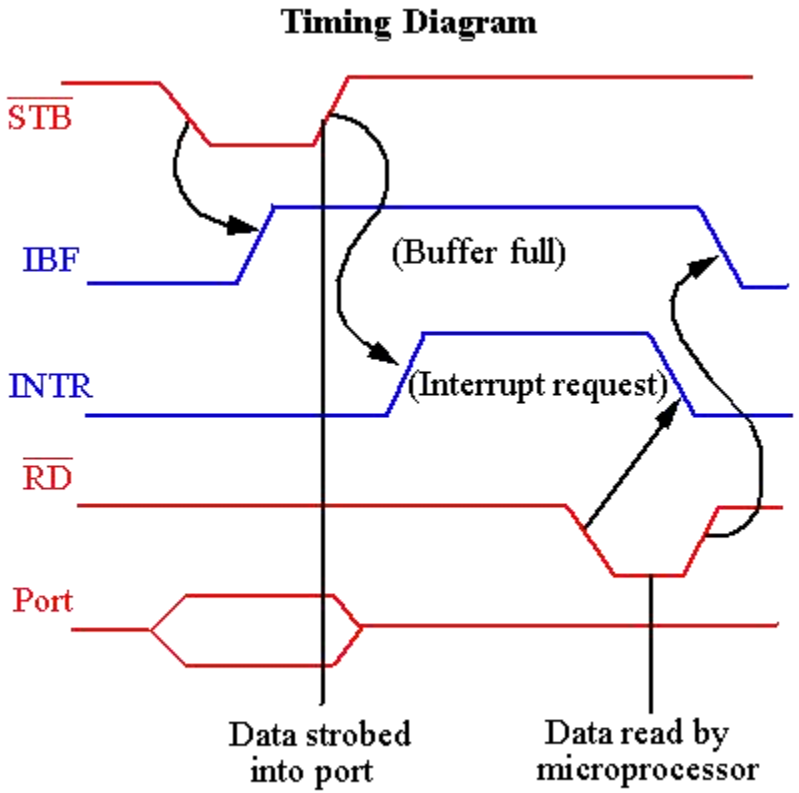
IFB **Input buffer full** is an output indicating that the input latch contain information

INTR **Interrupt request** is an output that requests an interrupt

INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.

PC7,PC6 The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.





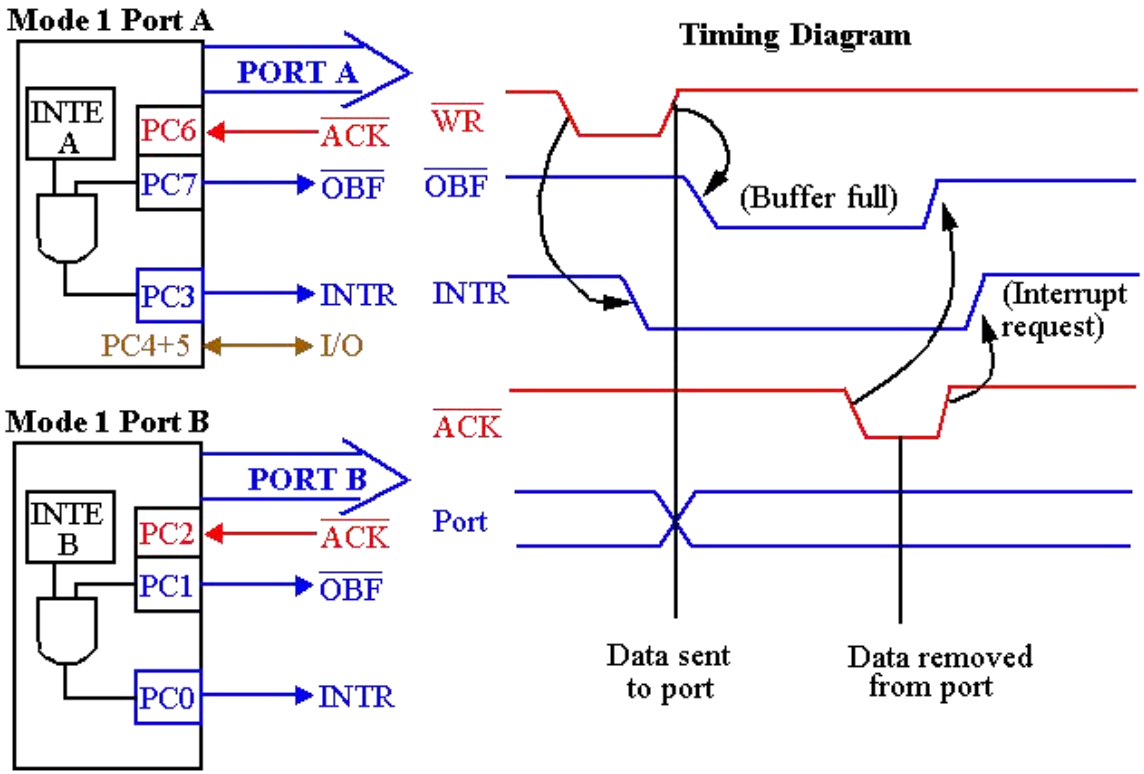
$\overline{\text{OBF}}$ **Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on $\overline{\text{ACK}}$.

$\overline{\text{ACK}}$ The **acknowledge** signal causes the $\overline{\text{OBF}}$ pin to return to 0. This is a response from an external device.

INTR **Interrupt request** is an output that requests an interrupt

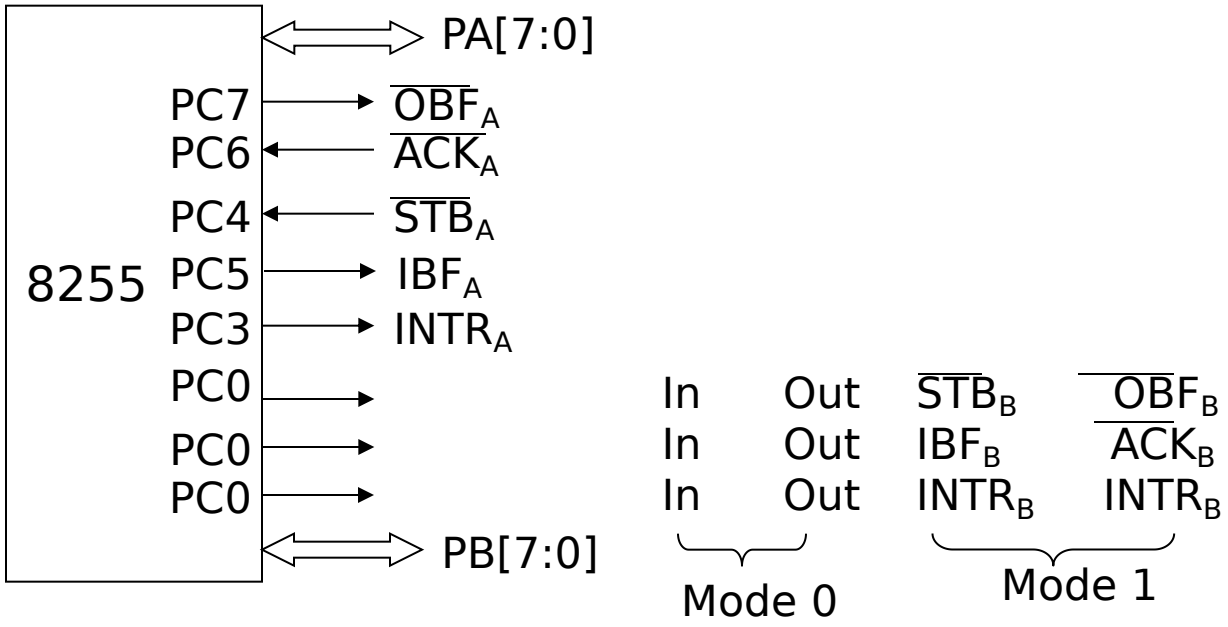
INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.

PC5,PC4 The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.



Programming 8255

- Mode 2:
  - — Port A is programmed to be bi-directional
  - — Port C is for handshaking
  - — Port B can be either input or output in mode 0 or mode 1



INTR — **Interrupt request** is an output that requests an interrupt

$\overline{\text{OBF}}$ — **Output buffer full** is an output indicating that the output buffer contains data for the bi-directional bus

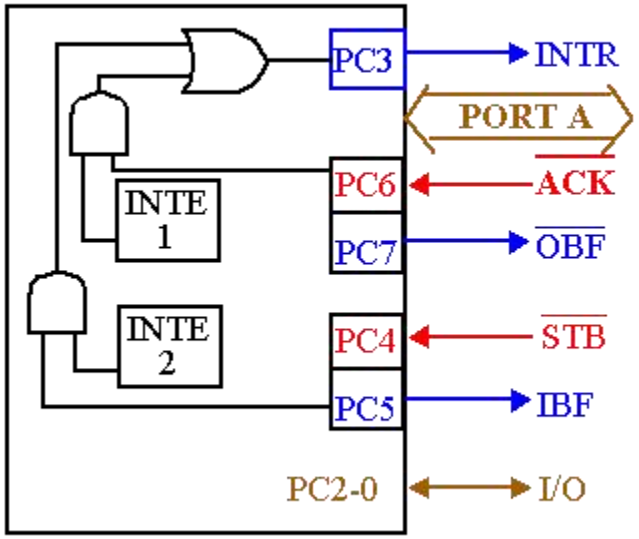
$\overline{\text{ACK}}$ — **Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state

$\overline{\text{STB}}$ — The strobe input loads data into the port A latch

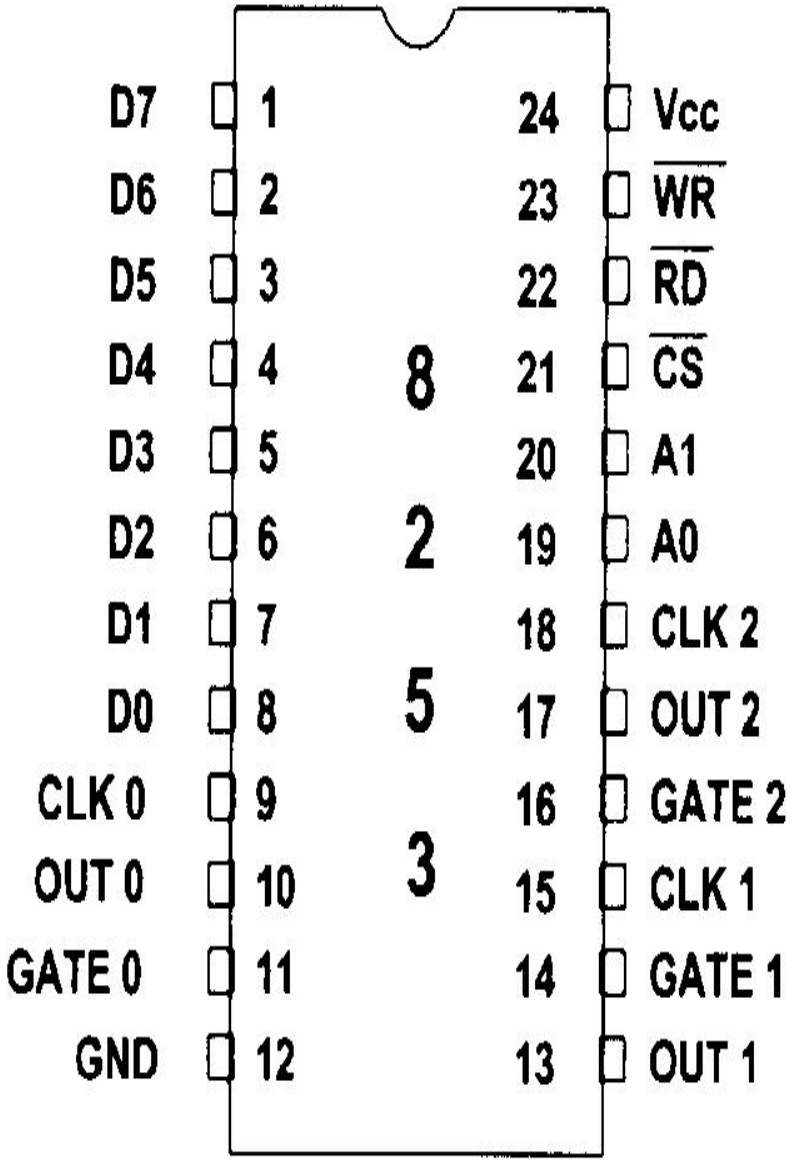
IFB — **Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus

INTE — **Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)

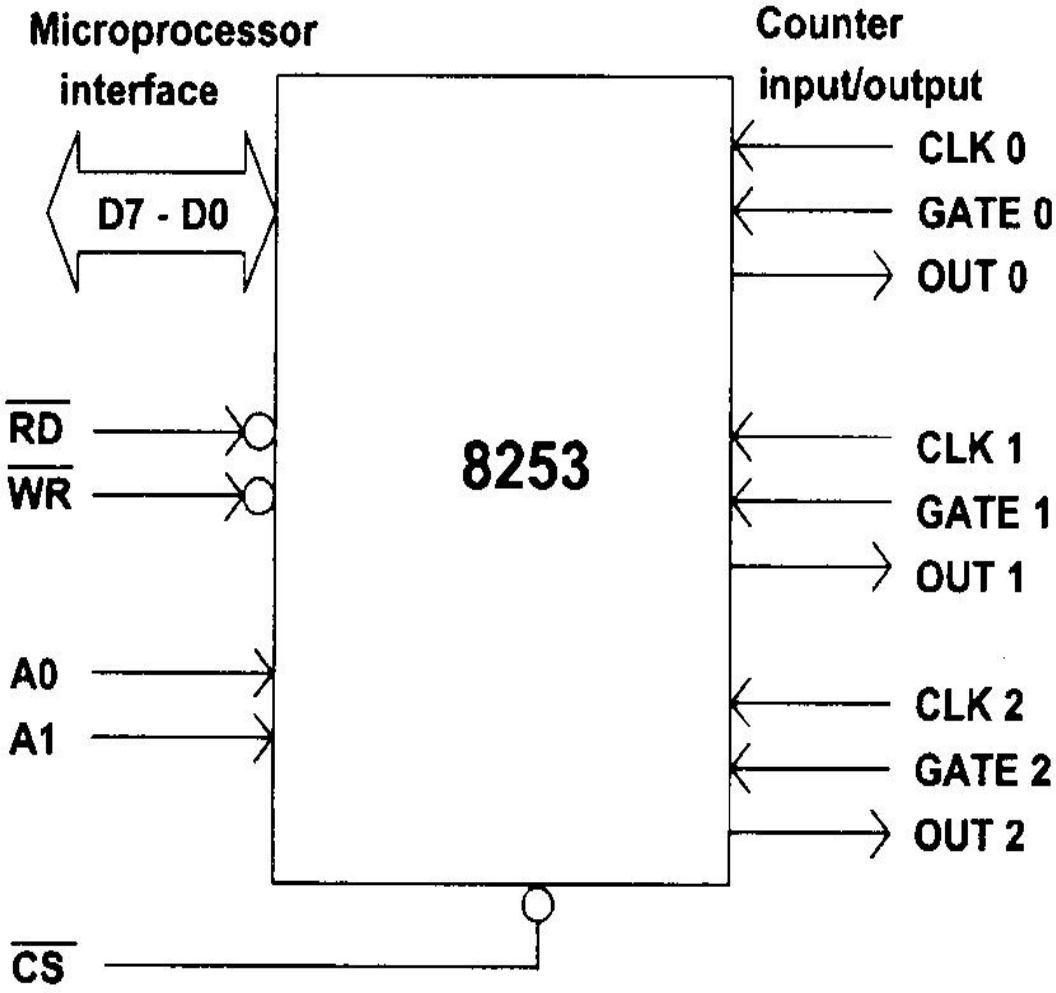
PC2,PC1 and PC0 — Theses port C pins are general-purpose I/O pins that are available for any purpose.



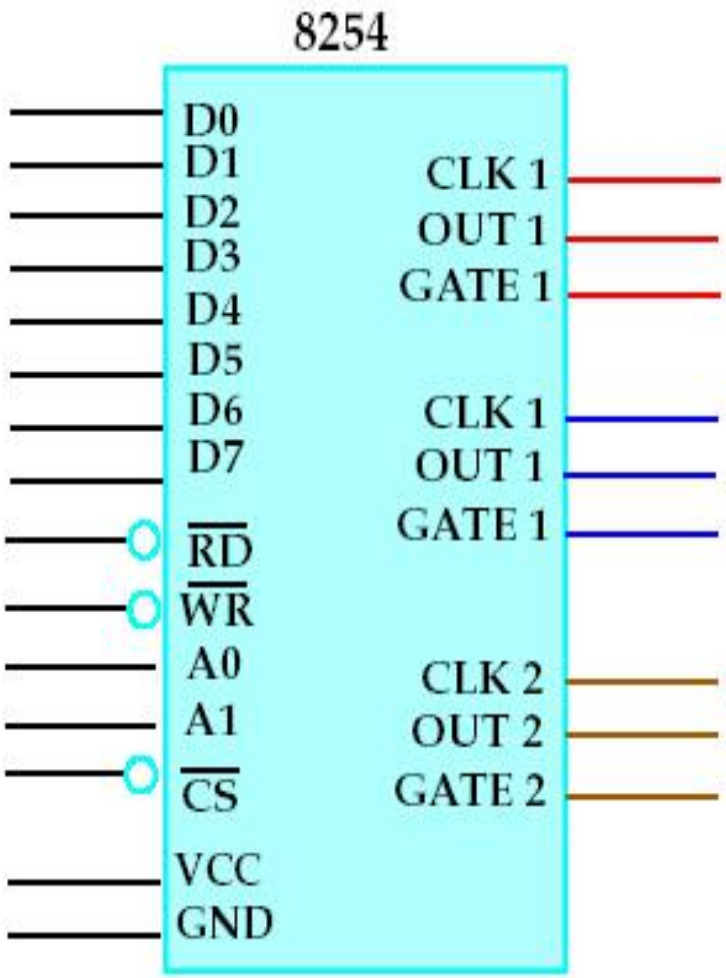
8253



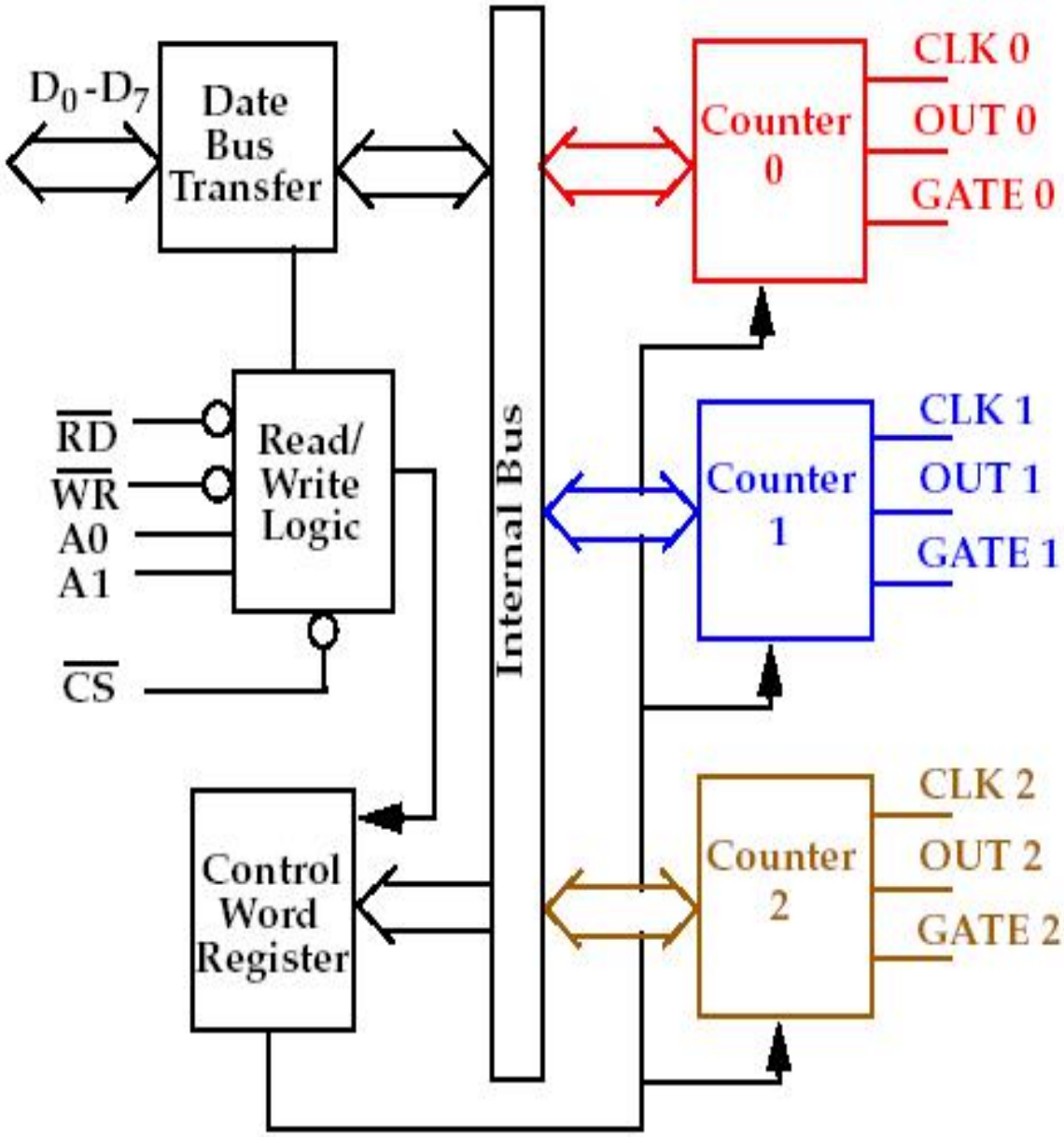
Block diagram



Pin-out



Internal structure



Counters:

Three Counters – C1,C2 & C3

Each 16 Bit Identical Presettable

Down Counter Operates In BCD /Hex

Controlled By Loading Count To Command Word Register

Control Logic:

$\overline{CS}$ – Logic 0 – Enables 8253

$\overline{RD}$ – Logic 0 – Tells Microprocessor Reads Count From 8253

WR – Logic 0 – Tells Microprocessor Writes Count/ Command Into 8253

Data Buffers:

8 Bit Bidirectional D0-D7 Connected To Data Bus Of Microprocessor

In Reads Data From Peripheral

Out Writes Data To Peripheral

Control Word Register:

Accepts 8 Bit Control Word Written By Microprocessor

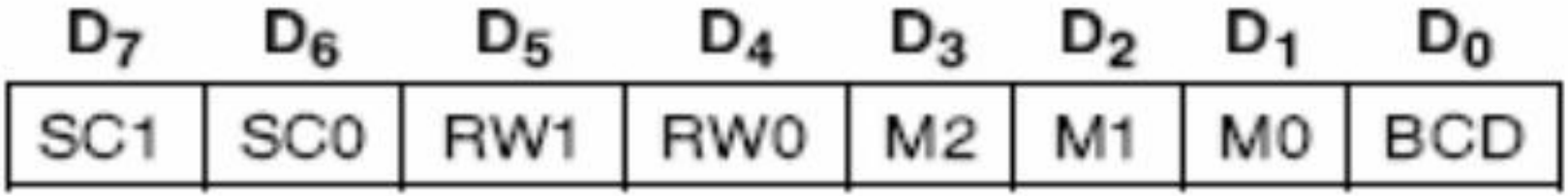
Can Only Be Written (Not Read)

Control Word Chooses One Of The Six Modes Of Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	OPERATION
0	1	0	0	0	**Write Counter** 0
0	1	0	0	1	**Write Counter** 1
0	1	0	1	0	**Write Counter** 2
0	1	0	1	1	**Write Control Word**
0	0	1	0	0	**Read Counter** 0
0	0	1	0	1	**Read Counter** 1
0	0	1	1	0	**Read Counter** 2
0	0	1	1	1	**No Operation (Tristated)**
0	1	1	**X**	**X**	**No Operation (Tristated)**
1	**X**	**X**	**X**	**X**	8253 **Not Selected**

Control Word

F



SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

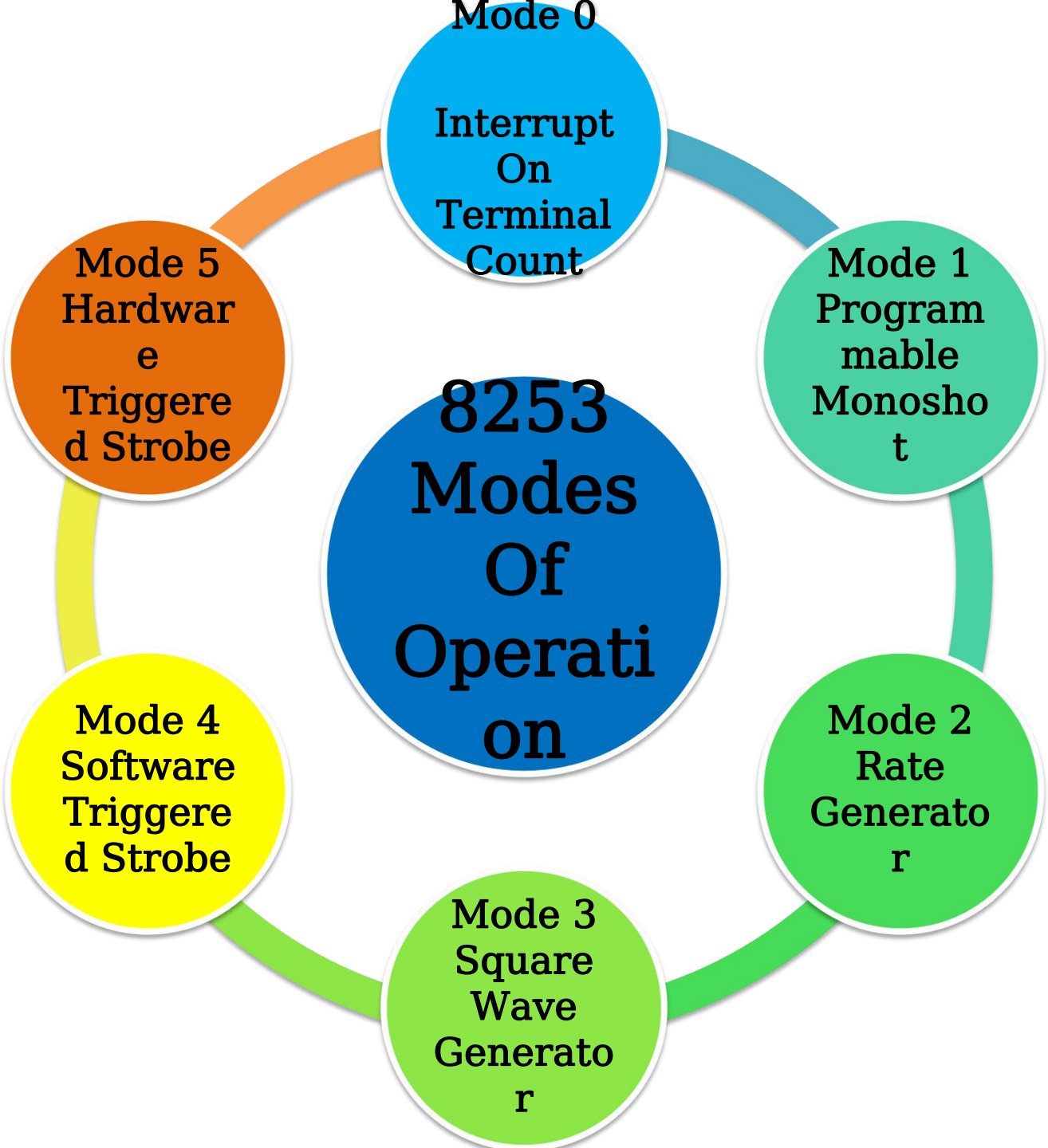
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)


8253 Modes Of Operation
Mode 0
Interrupt On Terminal Count
Mode 1 Programmable Monoshot
Mode 2 Rate Generator
Mode 3 Square Wave Generator
Mode 4 Software Triggered Strobe
Mode 5 Hardware Triggered Strobe

8254 Modes Of Operation

1.Mode 0 (Interrupt On Terminal Count)

2.Mode 1 (Programmable Monoshot)

3.Mode 2 (Rate Generator)

4.Mode 3 (Square Wave Generator)

5.Mode 4 (Software Triggered Strobe)

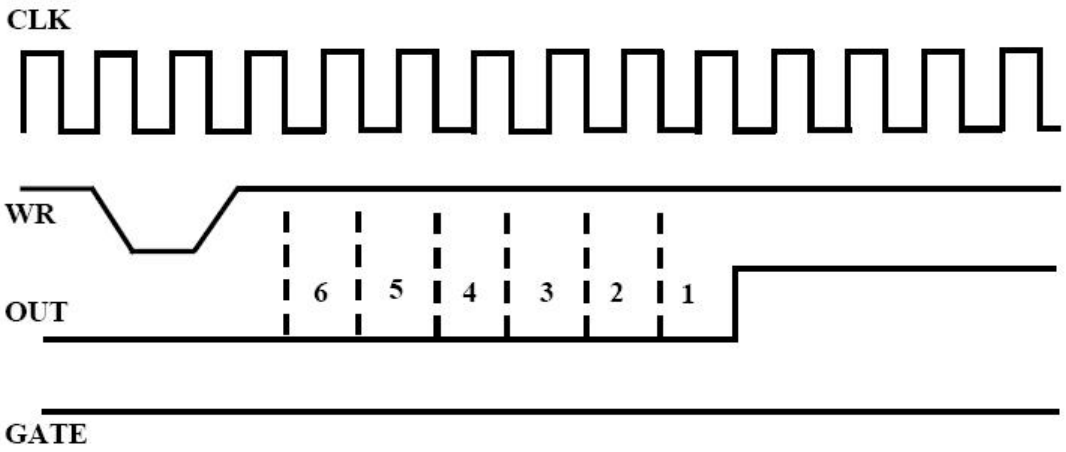
6.Mode 5 (Hardware Triggered Strobe)

Mode 0: Interrupt On Terminal Count

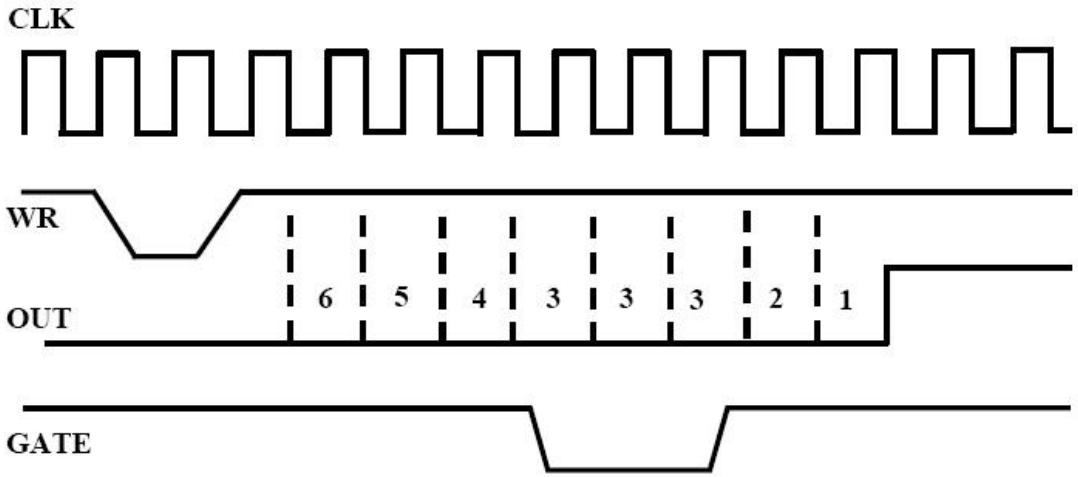
- The output goes high after the terminal count is reached. The counter stops if the Gate is low. The timer count register is loaded with a count (say 6) when the WR line is made low by the processor.

- The counter unit starts counting down with each clock pulse. The output goes high when the register value reaches zero. In the mean time if the GATE is made low the count is suspended at the value(3) till the GATE is enabled again.

Mode 0: Interrupt On Terminal Count



Mode 0 count when Gate is high (enabled)

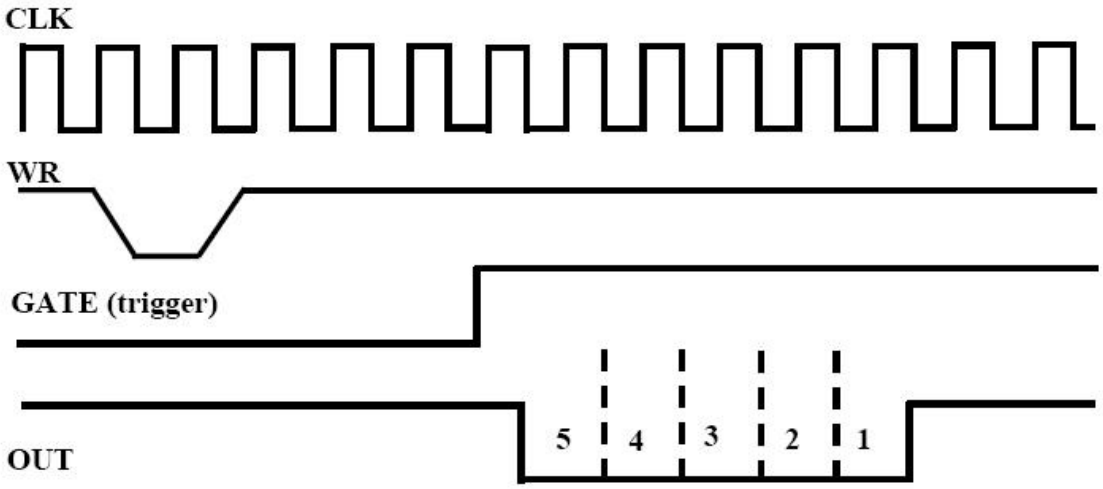


Mode 0 count when Gate is low temporarily (disabled)

Mode 1: Programmable mono-shot

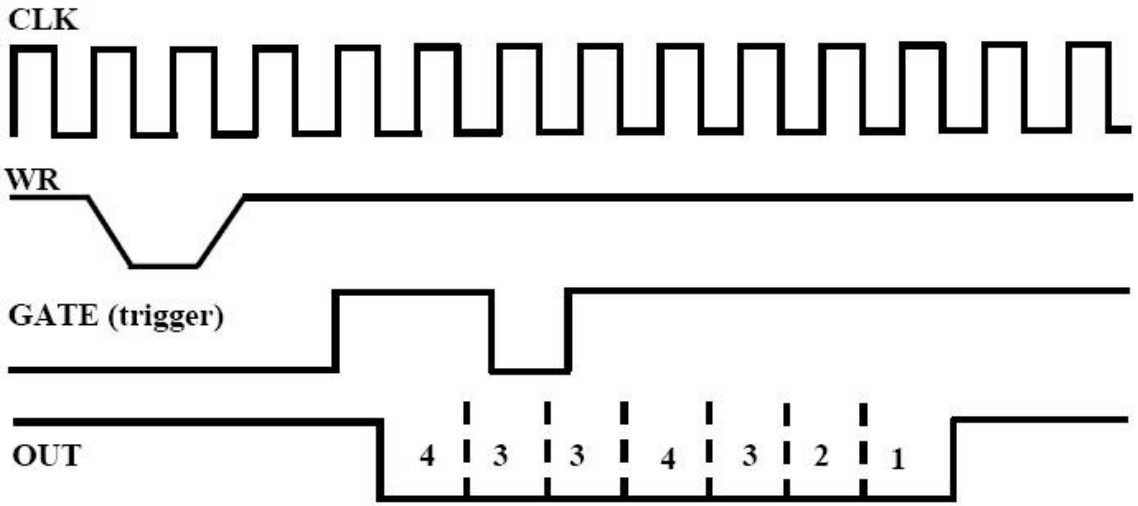
•The output goes low with the Gate pulse for a predetermined period depending on the counter. The counter is disabled if the GATE pulse goes momentarily low.

•The counter register is loaded with a count value as in the previous case (say 5) . The output responds to the GATE input and goes low for period that equals the count down period of the register (5 clock pulses in this period). By changing the value of this count the duration of the output pulse can be changed. If the GATE becomes low before the count down is completed then the counter will be suspended at that state as long as GATE is low Thus it works as a mono-shot.



Mode 1 the gate goes high. The output goes low for the period depending on the count.

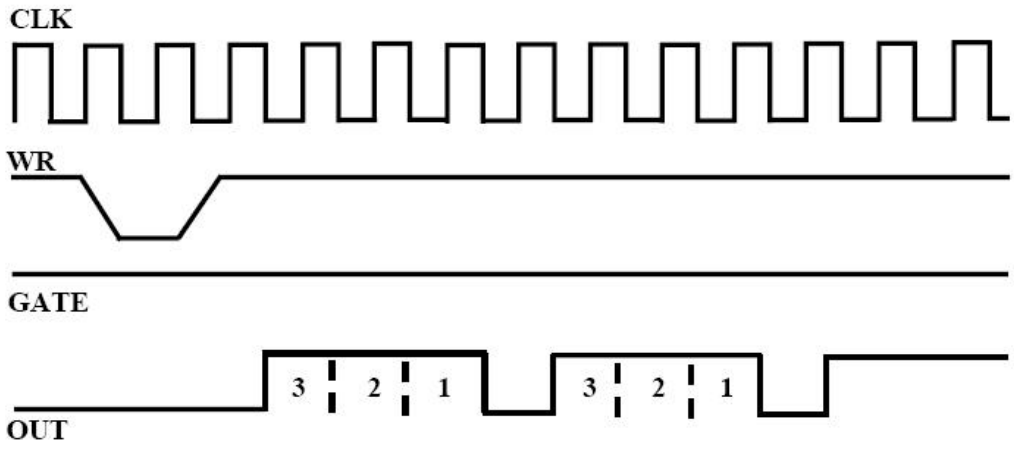
Mode 1 the gate pulse is disabled momentarily causing the counter to stop.



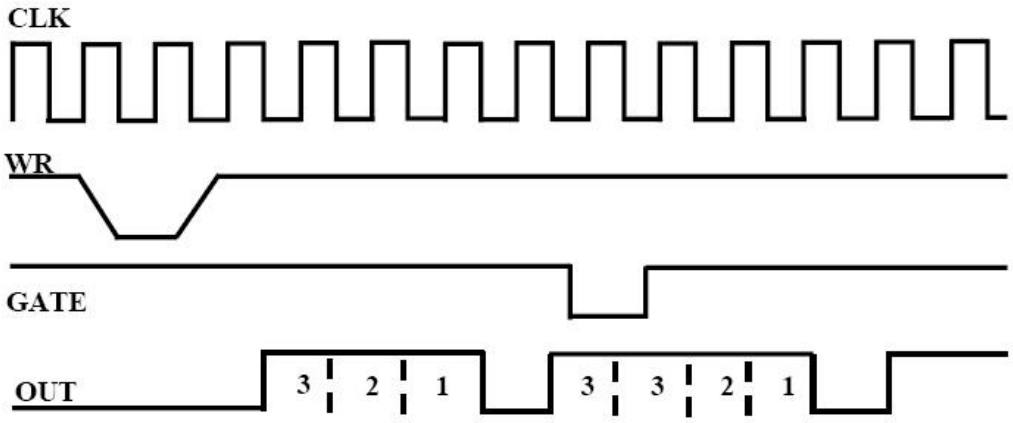
Mode 2: Rate Generator

In this mode it operates as a rate generator. The output goes high for a period that equals the time of count down of the count register (3 in this case). The output goes low exactly for one clock period before it becomes high again. This is a periodic operation.

Mode 2: Rate Generator



Mode 2 Operation when the GATE is kept high

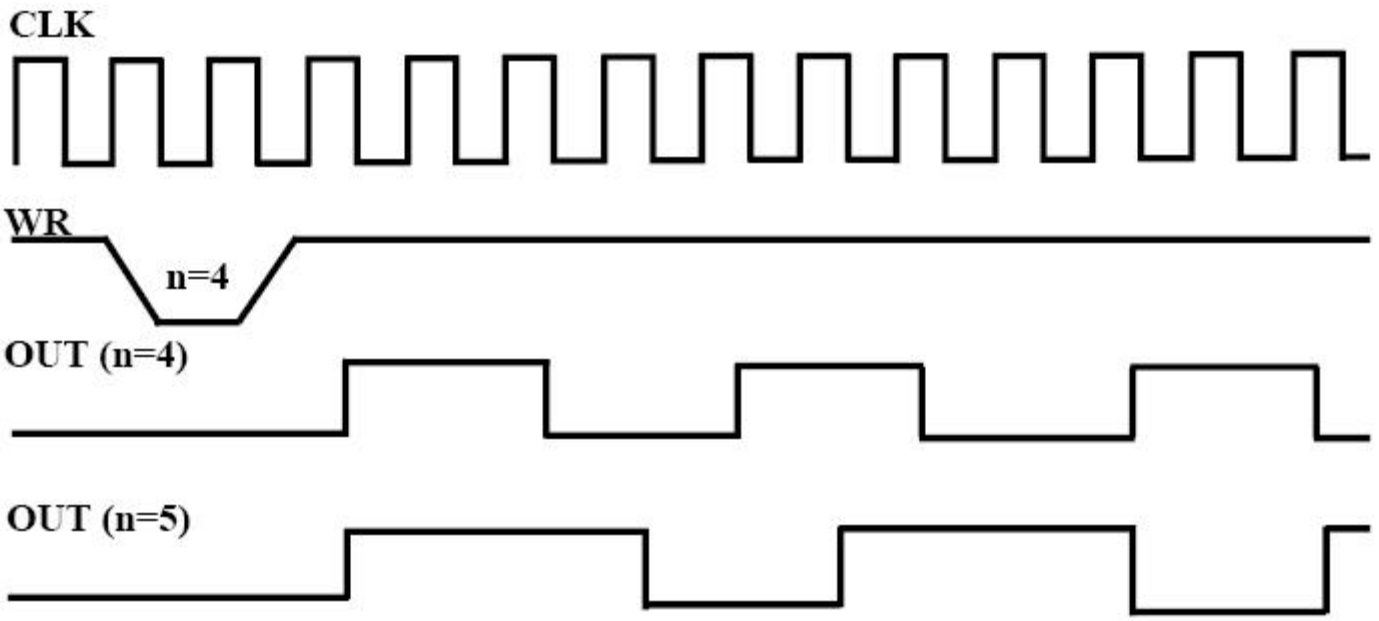


Mode 2 operation when the GATE is disabled momentarily.

Mode 3: SQUARE WAVE RATE GENERATOR

It is similar to Mode 2 but the output high and low period is symmetrical. The output goes high after the count is loaded and it remains high for period which equals the count down period of the counter register. The output subsequently goes low for an equal period and hence generates a symmetrical square wave unlike Mode 2.

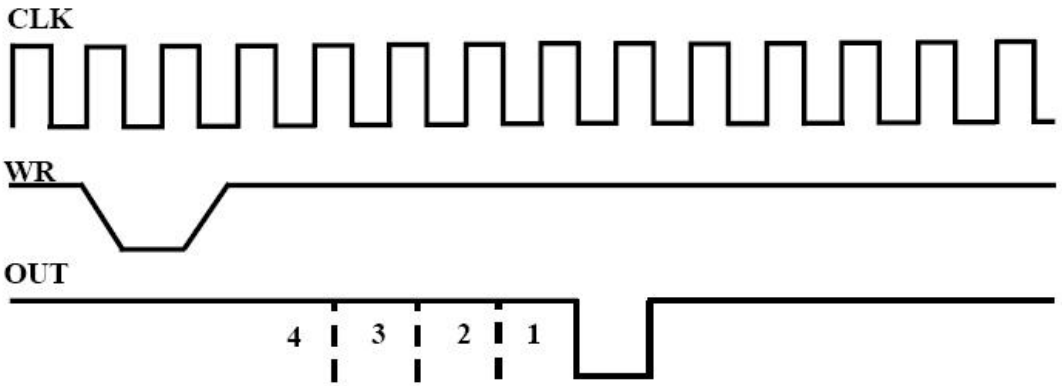
Mode 3: Square Wave Generator



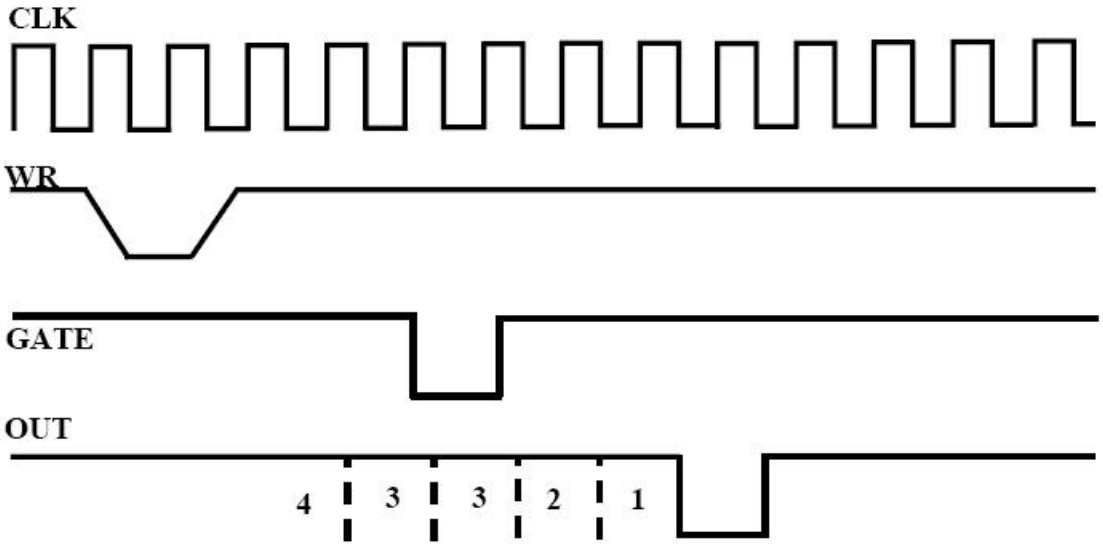
Mode3 Operation: Square Wave generator

Mode 4: Software triggered Strobe

In this mode after the count is loaded by the processor the count down starts. The output goes low for one clock period after the count down is complete. The count down can be suspended by making the GATE low. This is also called a software triggered strobe as the count down is initiated by a program.



Mode 4 Software Triggered Strobe when GATE is high

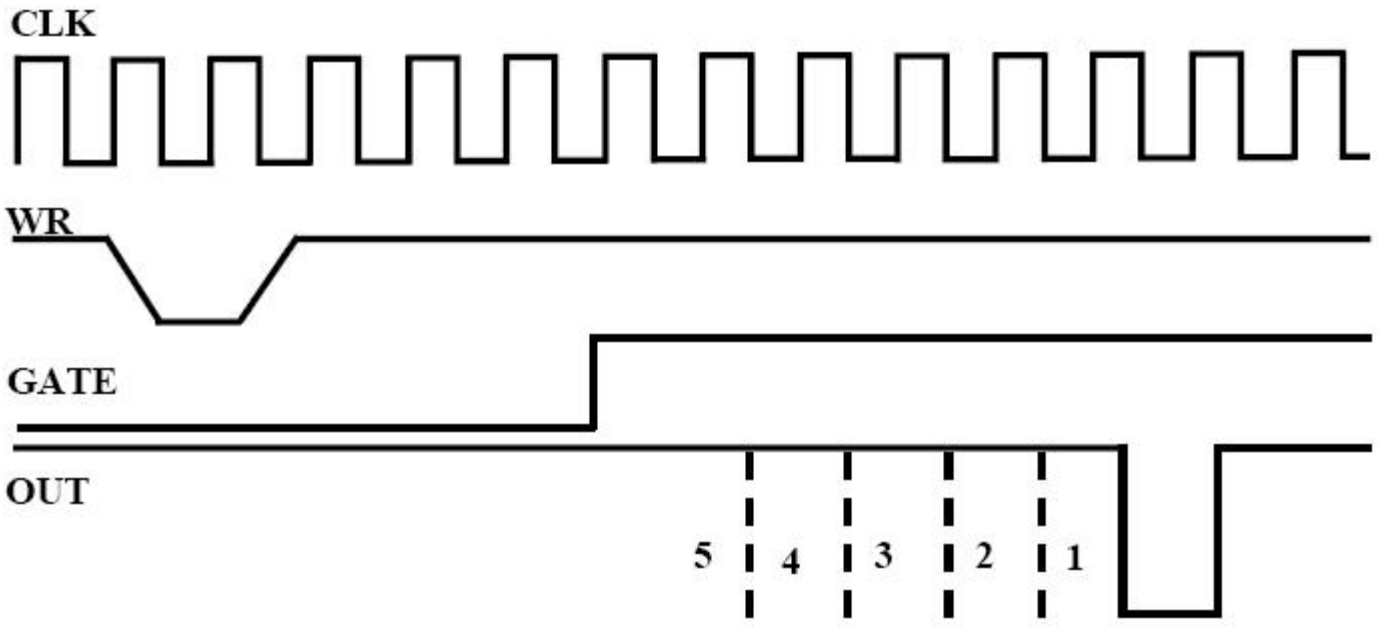


Mode 4 Software Triggered Strobe when GATE is momentarily low

Mode 5: Hardware triggered Strobe

The count is loaded by the processor but the count down is initiated by the GATE pulse. The transition from low to high of the GATE pulse enables count down. The output goes low for one clock period after the count down is complete

Mode 5: Hardware triggered Strobe



Mode 5 Hardware Triggered Strobe

8259

Programmable Interrupt Controller (PIC)

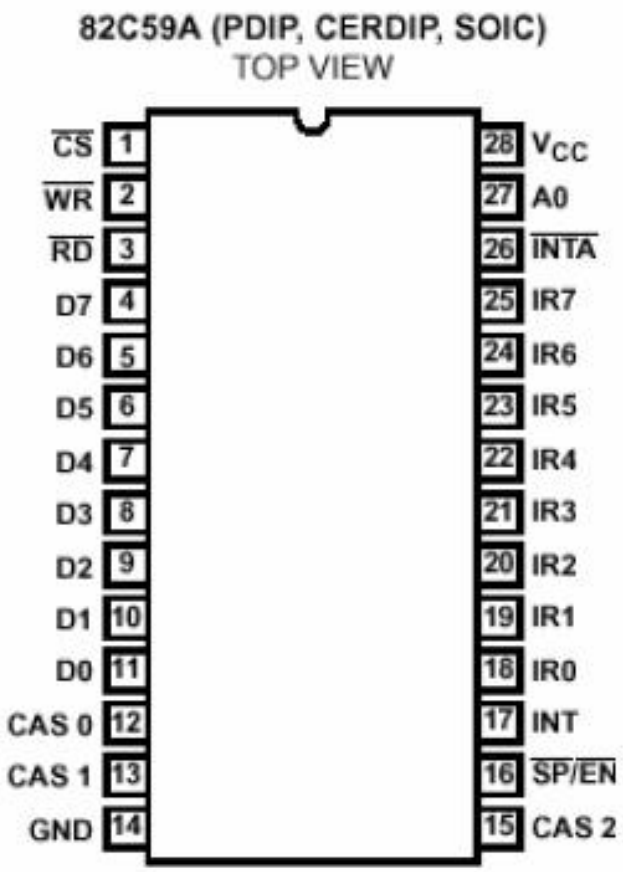
1. This IC is designed to simplify the implementation of the interrupt interface in the 8088 and 8086 based microcomputer systems.
2. The operation of the PIC is programmable under software control (Programmable)and it can be configured for a wide variety of applications.
3. 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor.
4. This controller can be expanded without additional hardware to accept up to 64 interrupt request inputs. This expansion required a master 8259A and eight 8259A slaves.
5. Some of its programmable features are:

· The ability to accept level-triggered or edge-triggered inputs.

· The ability to be easily cascaded to expand from 8 to 64 interrupt-inputs.

· Its ability to be configured to implement a wide variety of

Pin – Diagram 8259



PIN	DESCRIPTION
D7 - D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS 2 - CAS 0	Cascade Lines
$\overline{SP/EN}$	Slave Program Input Enable
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 - IR7	Interrupt Request Inputs

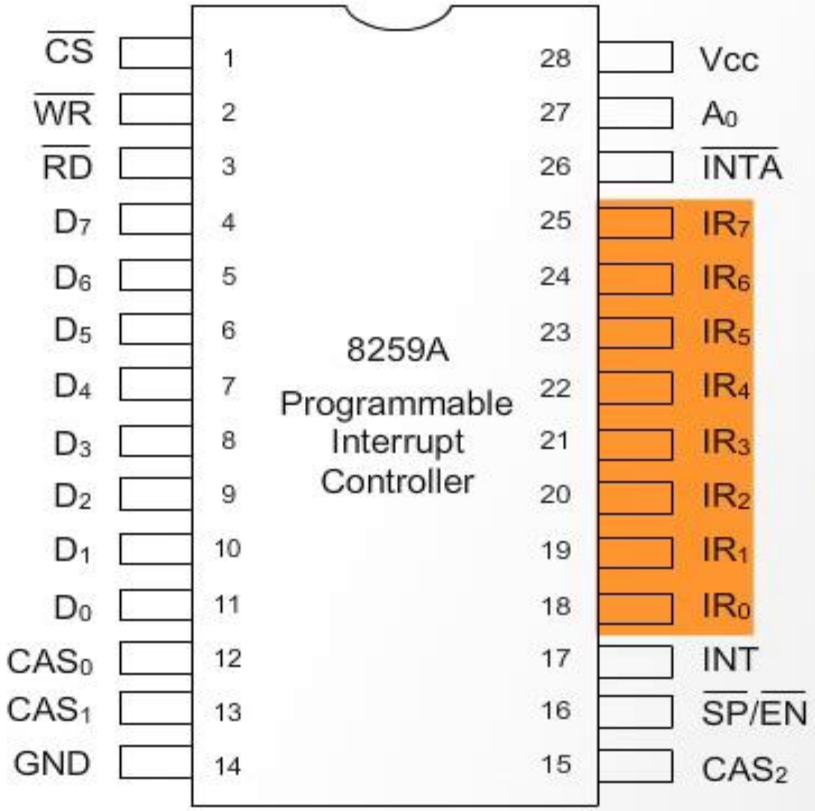
Pin Assignment

1. **D7- D0** is connected to microprocessor data bus D7-D0 (AD7-AD0).
2. **IR7- IR0**, Interrupt Request inputs are used to request an interrupt and to connect to a slave in a system with multiple 8259As.
3. **WR -** the write input connects to write strobe signal of microprocessor.
4. **RD -** the read input connects to the IORC signal.
5. **INT -** the interrupt output connects to the INTR pin on the microprocessor from the master, and is connected to a master IR pin on a slave.
6. **INTA -** the interrupt acknowledge is an input that connects to the INTA signal on the system. In a system with a master and slaves, only the master INTA signal is connected.
7. **A0** - this address input selects different command words within the 8259A.

Pin Assignment

- When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
- When the 8259A is not in buffered mode, this pin programs the device as a master (1) or a slave (0).
- CAS2-CAS0, the cascade lines are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

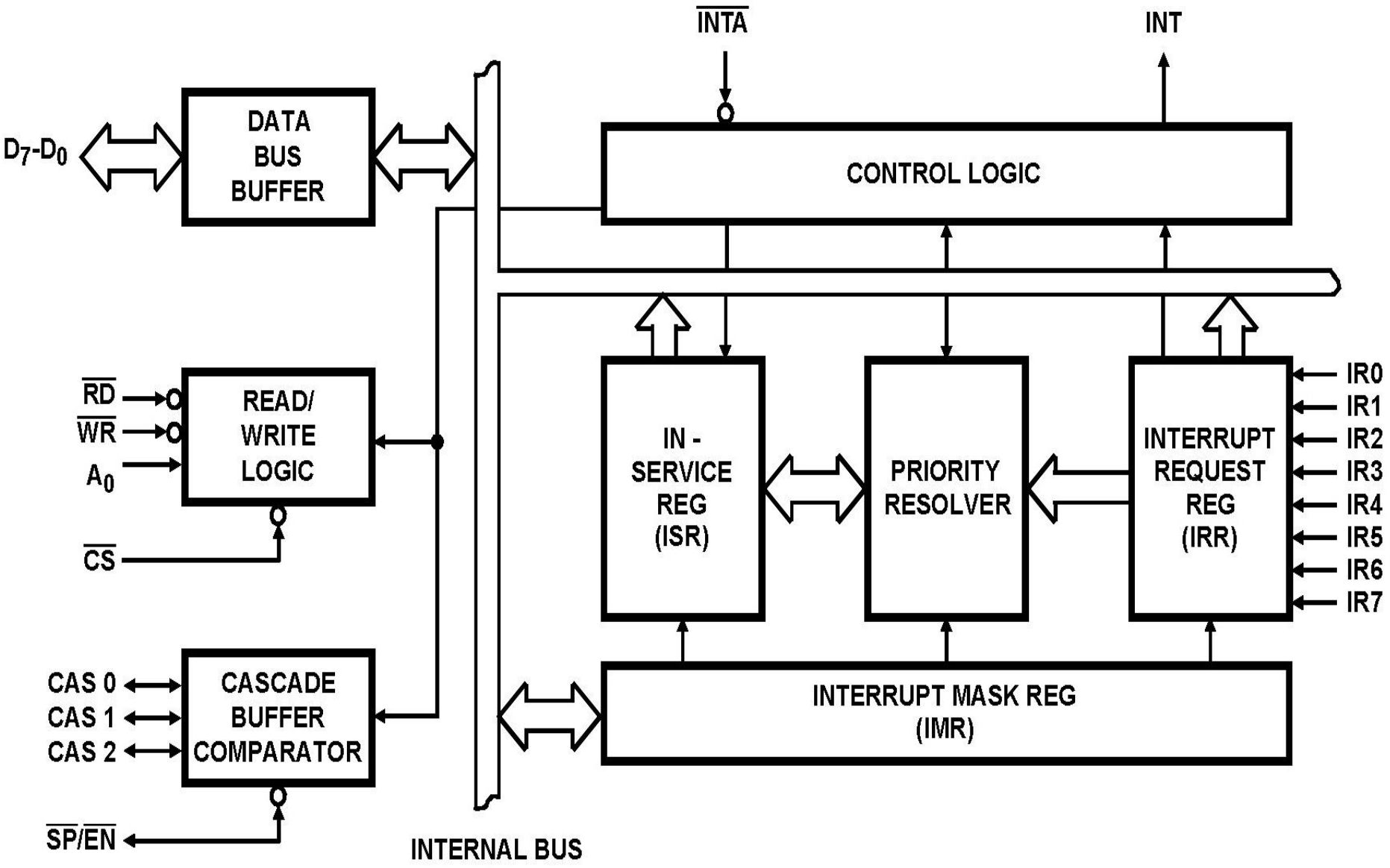
8259 PIC



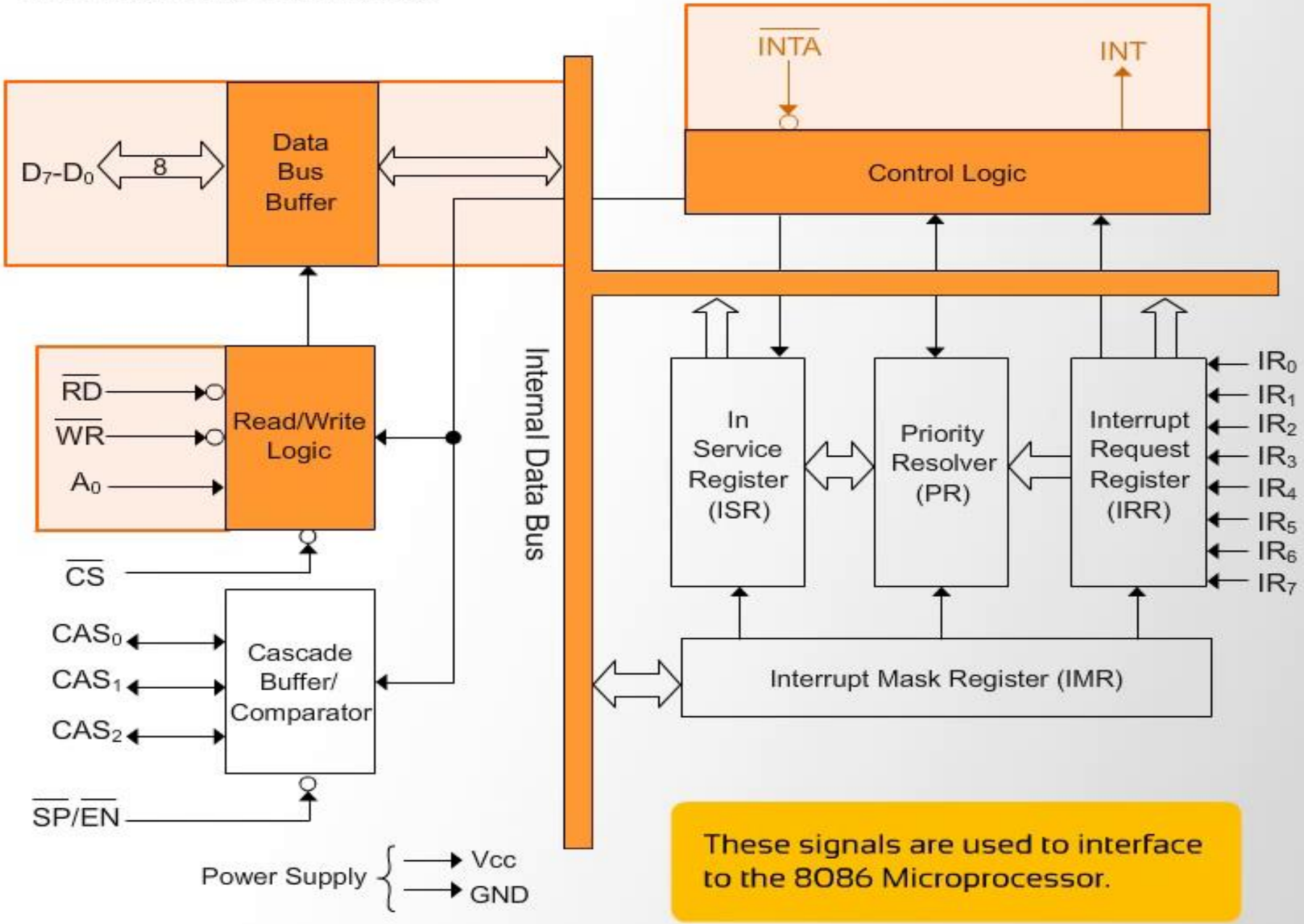
Upto eight Hardware Interrupting devices are supported.

The processor is interrupted whenever the Interrupting device delivers a signal to the 8259.

8259A PIC- BLOCK DIAGRAM

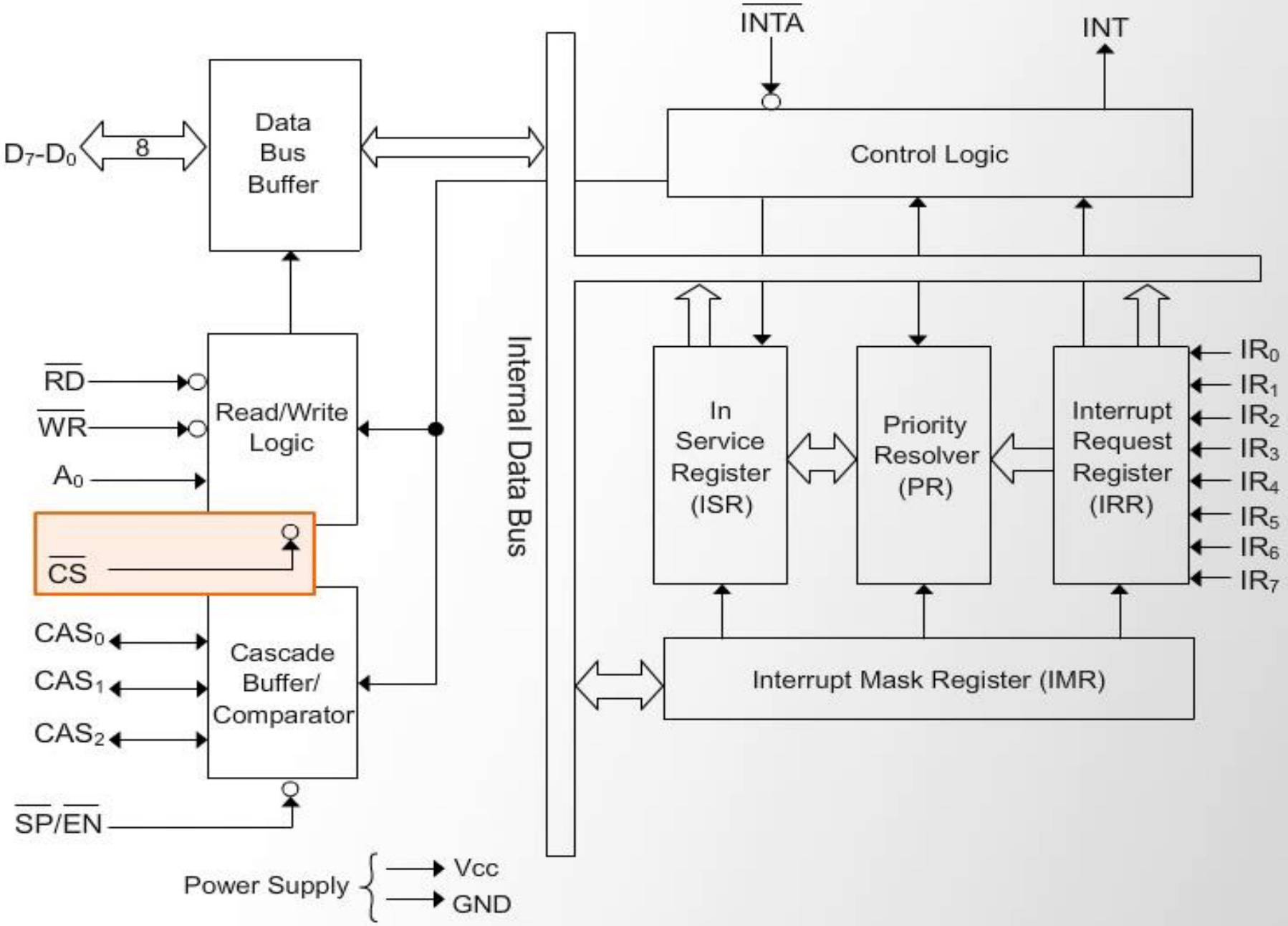


The Internals of 8259

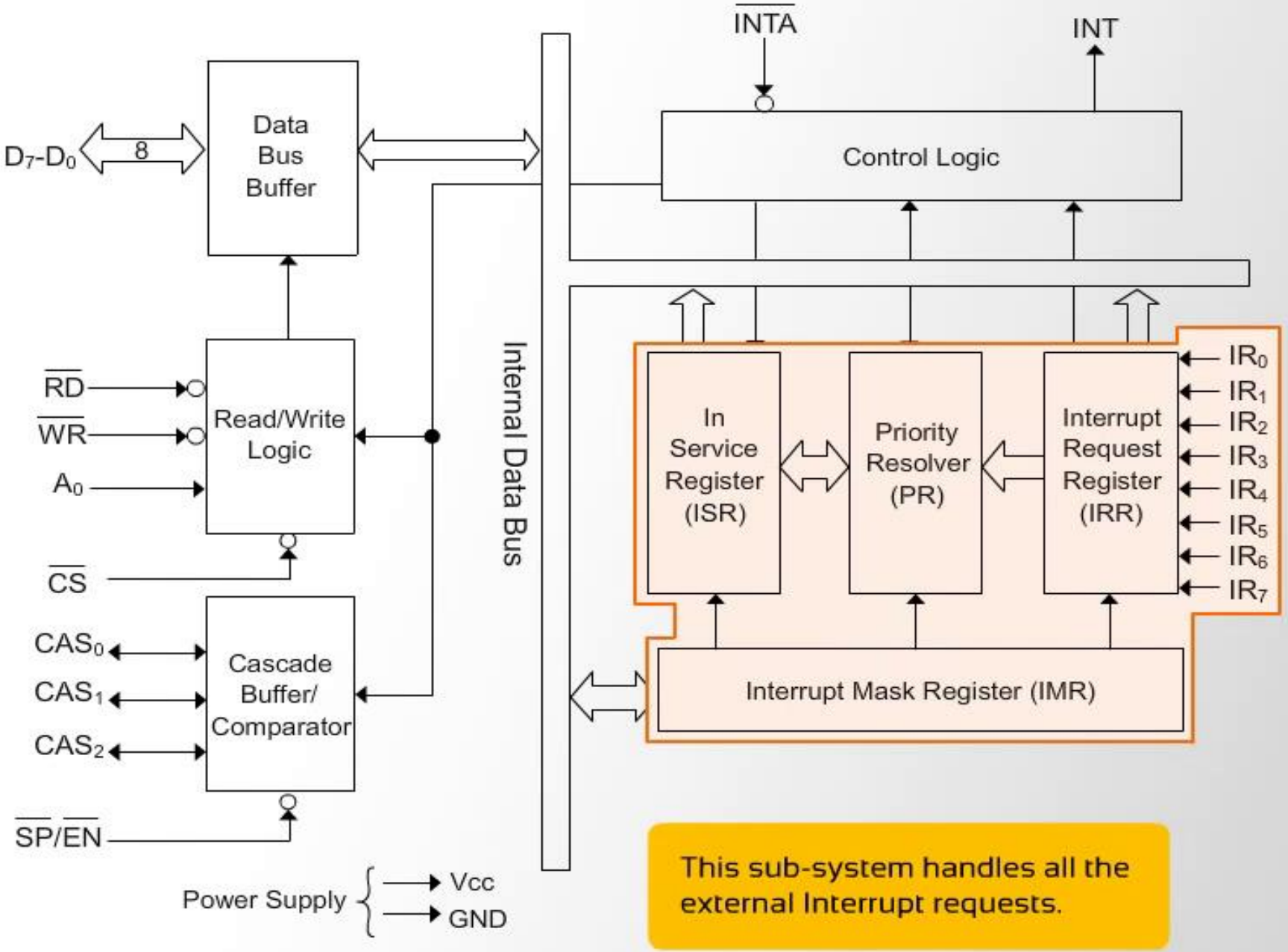


These signals are used to interface to the 8086 Microprocessor.

The Internals of 8259

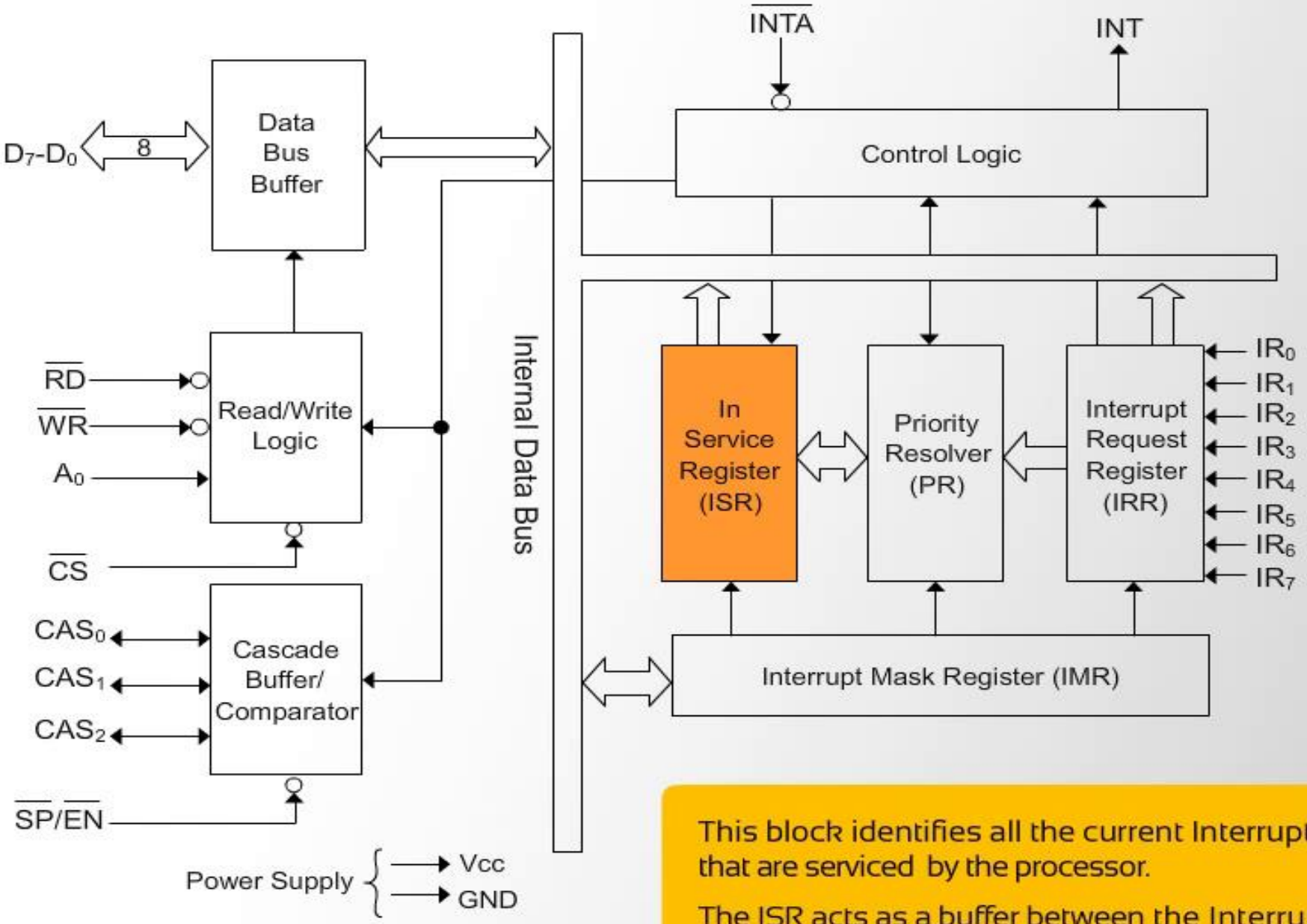


The Internals of 8259



This sub-system handles all the external Interrupt requests.

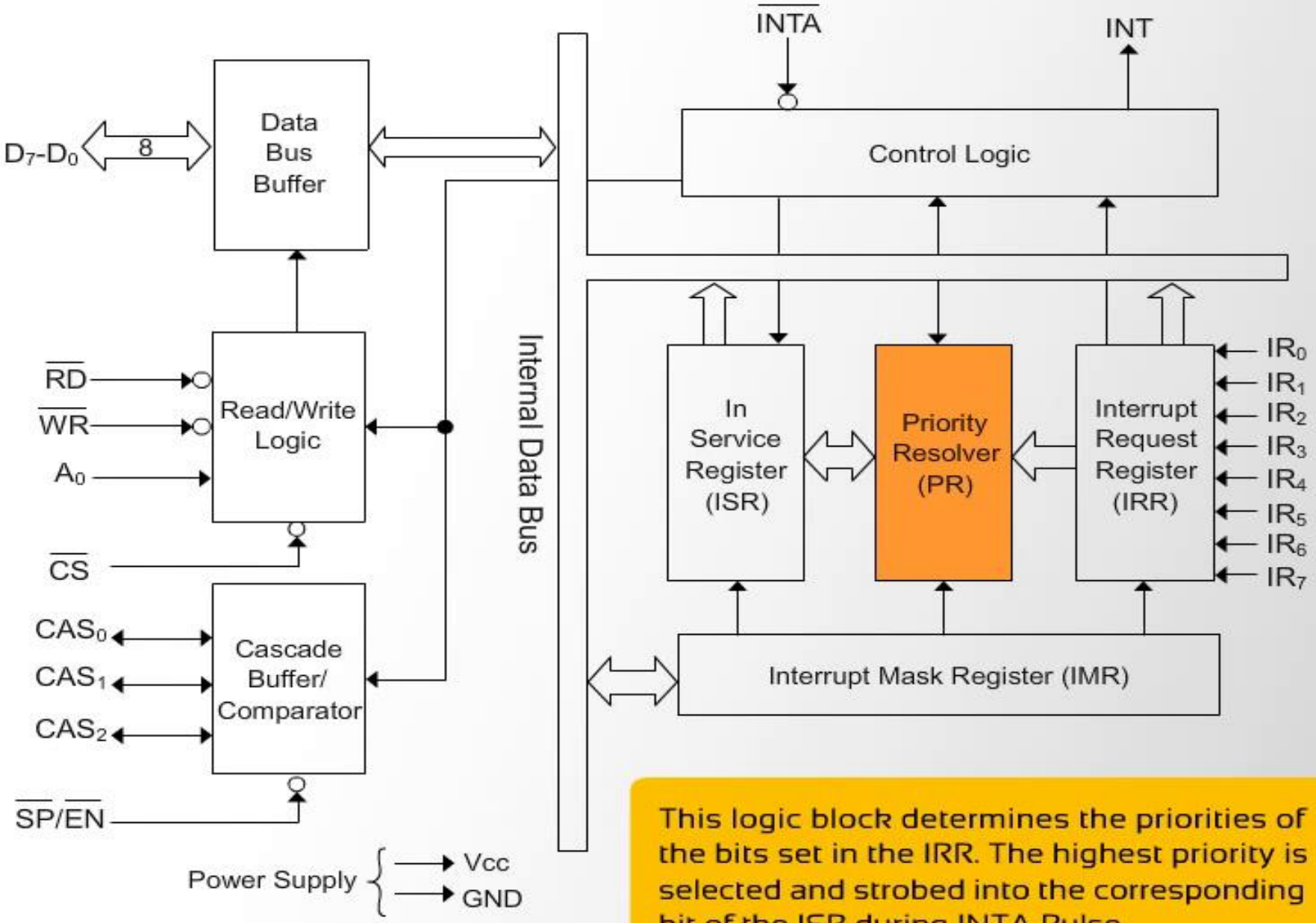
The Internals of 8259



This block identifies all the current Interrupts that are serviced by the processor.

The ISR acts as a buffer between the Interrupt Request Register and the 8086.

The Internals of 8259



This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during INTA Pulse.