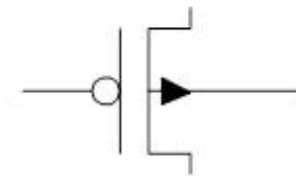
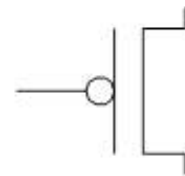
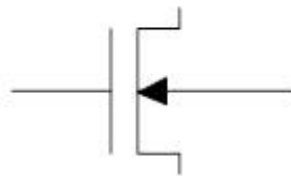
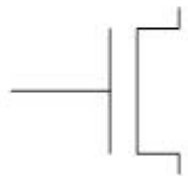


VLSI Design (EC0604)
Unit-1
**B.Tech (Electronics and
Communication)**
Semester-6
Ankur Changela

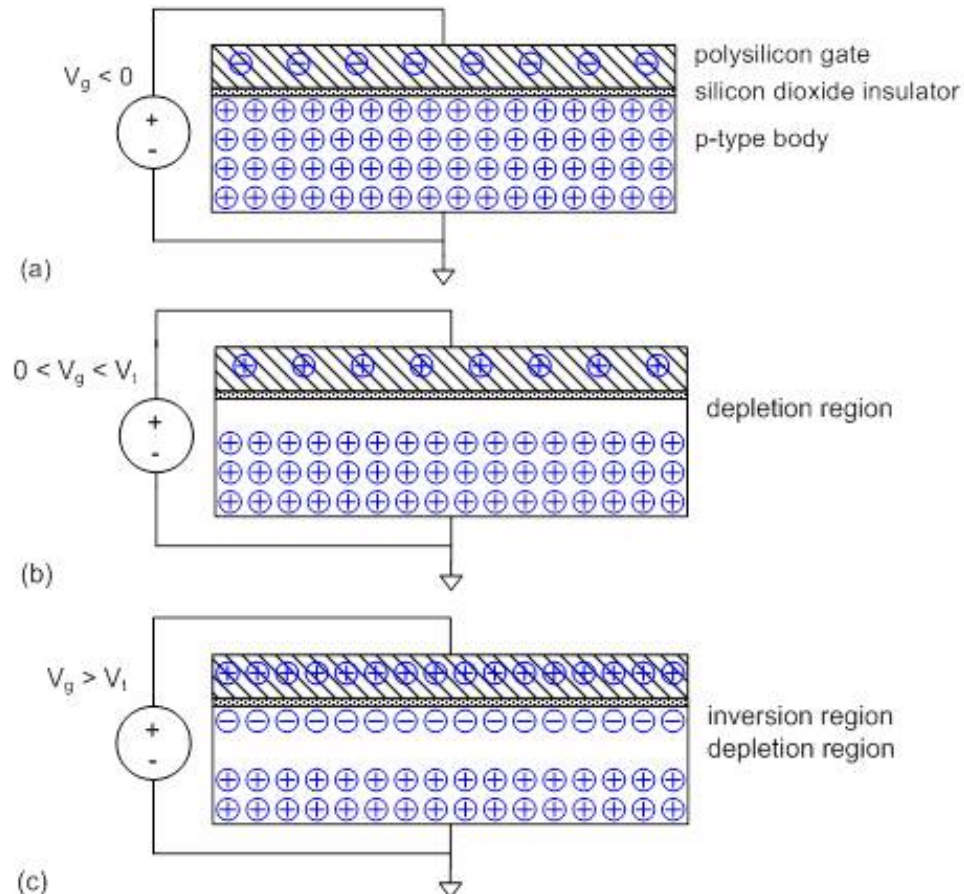
Introduction

- ❑ So far, we have treated transistors as ideal switches
- ❑ An ON transistor passes a finite amount of current
 - Depends on terminal voltages
 - Derive current-voltage (I-V) relationships
- ❑ Transistor gate, source, drain all have capacitance
 - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C / I) \Delta V$
 - Capacitance and current determine speed



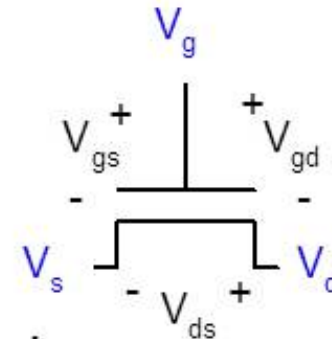
MOS Capacitor

- ❑ Gate and body form MOS capacitor
- ❑ Operating modes
 - Accumulation
 - Depletion
 - Inversion



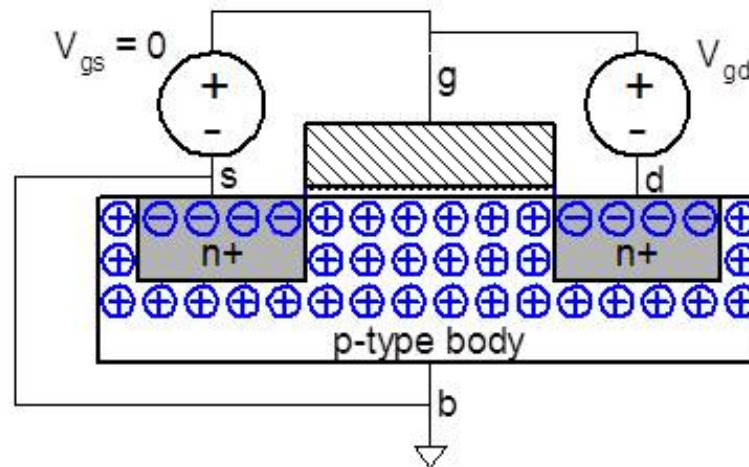
Terminal Voltages

- ❑ Mode of operation depends on V_g , V_d , V_s
 - $V_{gs} = V_g - V_s$
 - $V_{gd} = V_g - V_d$
 - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- ❑ Source and drain are symmetric diffusion terminals
 - By convention, source is terminal at lower voltage
 - Hence $V_{ds} \geq 0$
- ❑ nMOS body is grounded. First assume source is 0 too.
- ❑ Three regions of operation
 - *Cutoff*
 - *Linear*
 - *Saturation*



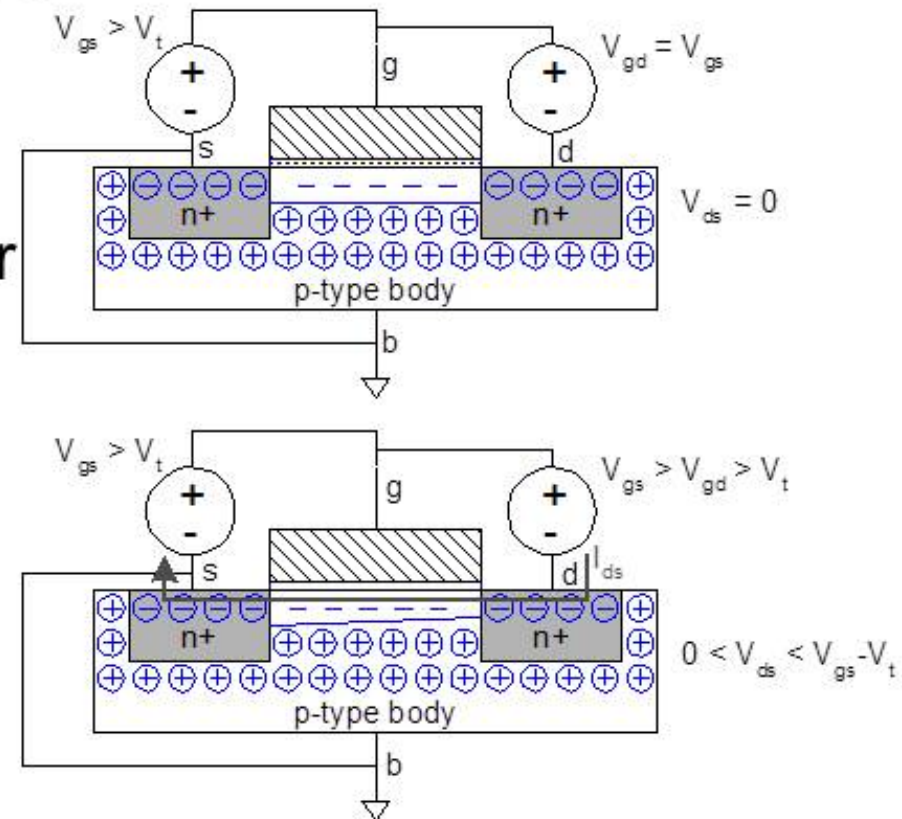
nMOS Cutoff

- ❑ No channel
- ❑ $I_{ds} \approx 0$



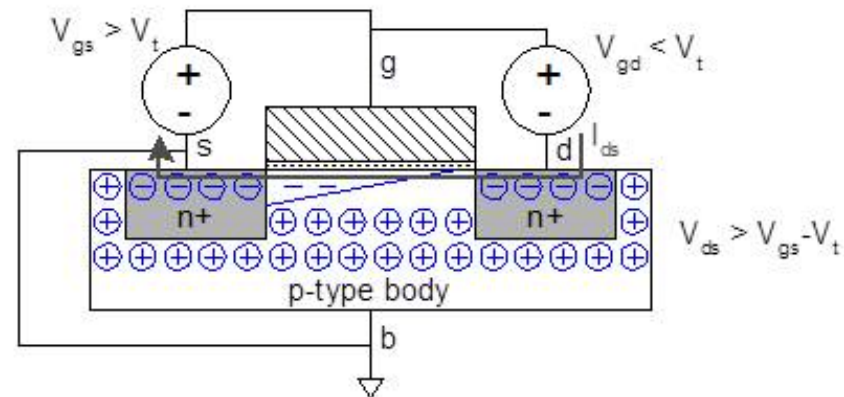
nMOS Linear

- ❑ Channel forms
- ❑ Current flows from d to s
 - e^- from s to d
- ❑ I_{ds} increases with V_{ds}
- ❑ Similar to linear resistor



nMOS Saturation

- ❑ Channel pinches off
- ❑ I_{ds} independent of V_{ds}
- ❑ We say current *saturates*
- ❑ Similar to current source



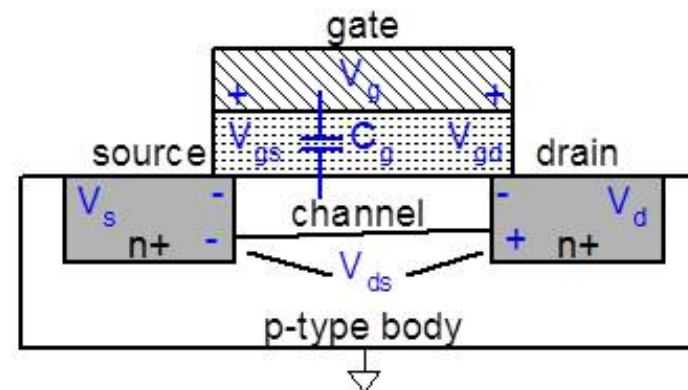
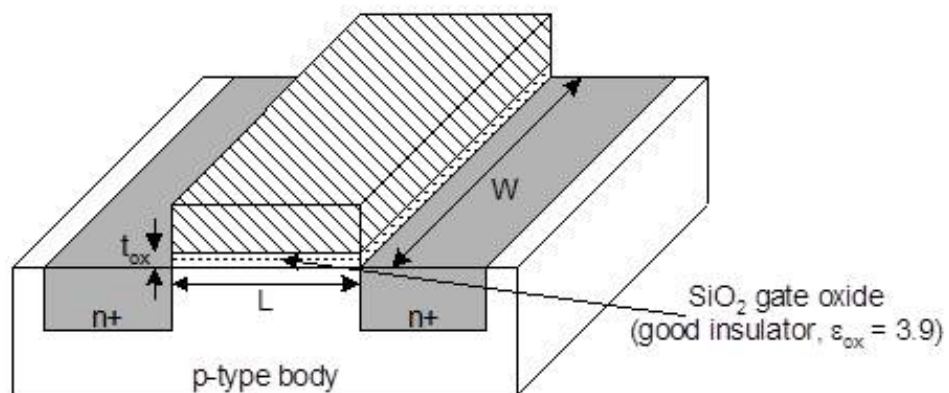
I-V Characteristics

- ❑ In Linear region, I_{ds} depends on
 - How much charge is in the channel?
 - How fast is the charge moving?

Channel Charge

- ❑ MOS structure looks like parallel plate capacitor while operating in inversions
 - Gate – oxide – channel
- ❑ $Q_{\text{channel}} = CV$
- ❑ $C = C_g = \epsilon_{\text{ox}} WL / t_{\text{ox}} = C_{\text{ox}} WL$
- ❑ $V = V_{\text{gc}} - V_t = (V_{\text{gs}} - V_{\text{ds}}/2) - V_t$

$$C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$$



Carrier velocity

- ❑ Charge is carried by e-
- ❑ Electrons are propelled by the lateral electric field between source and drain
 - $E = V_{ds}/L$
- ❑ Carrier velocity v proportional to lateral E-field
 - $v = \mu E$ μ called mobility
- ❑ Time for carrier to cross channel:
 - $t = L / v$

nMOS Linear I-V

- Now we know
 - How much charge Q_{channel} is in the channel
 - How much time t each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \quad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
 - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$$
$$= \frac{\beta}{2} (V_{gs} - V_t)^2$$

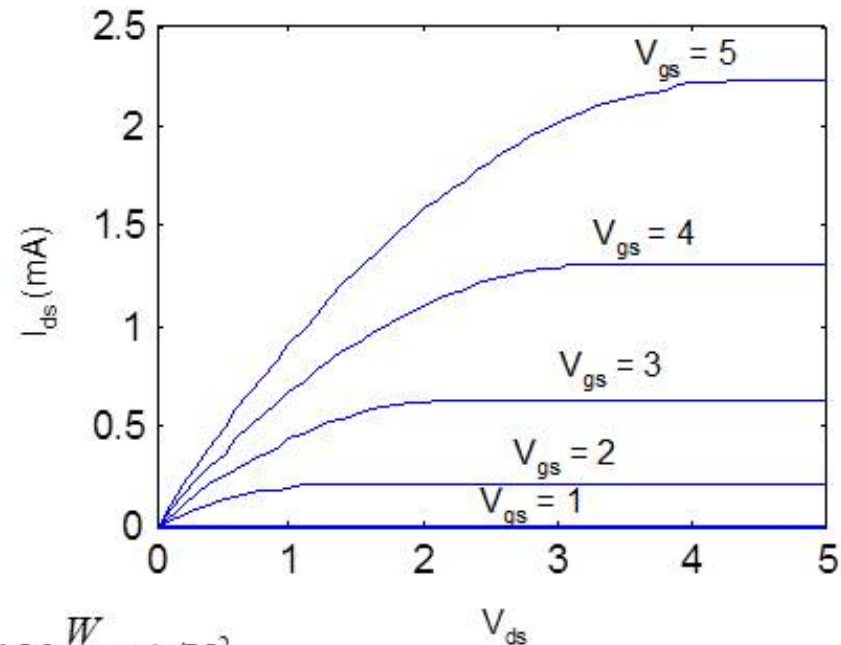
nMOS I-V Summary

- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

Example

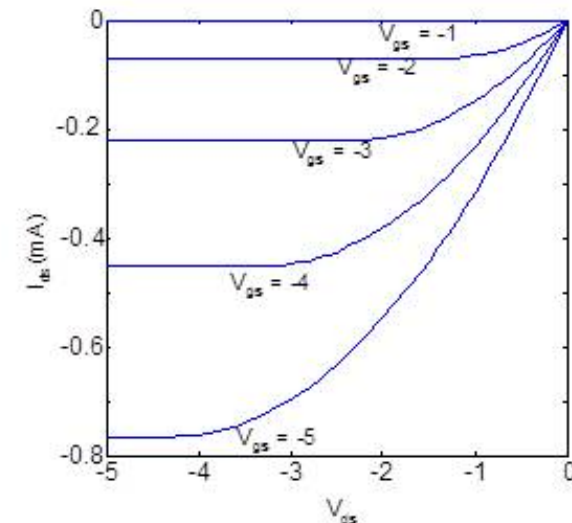
- We will be using a 0.6 μm process for your project
 - From AMI Semiconductor
 - $t_{\text{ox}} = 100 \text{ \AA}$
 - $\mu = 350 \text{ cm}^2/\text{V}^*\text{s}$
 - $V_t = 0.7 \text{ V}$
- Plot I_{ds} vs. V_{ds}
 - $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$
 - Use $W/L = 4/2 \lambda$



$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left(\frac{3.9 \times 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left(\frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

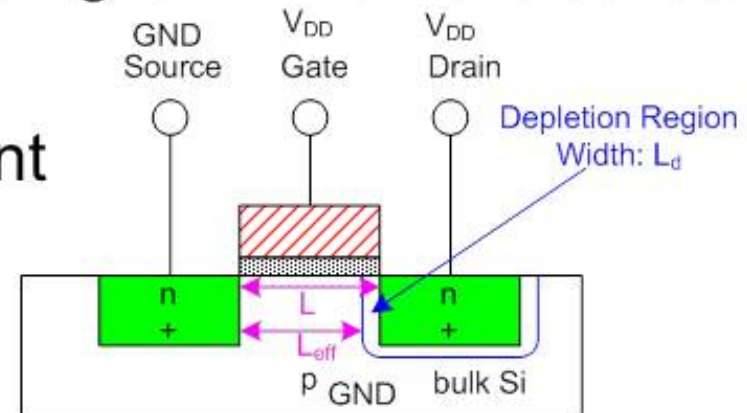
pMOS I-V

- ❑ All dopings and voltages are inverted for pMOS
 - Source is the more positive terminal
- ❑ Mobility μ_p is determined by holes
 - Typically 2-3x lower than that of electrons μ_n
 - 120 cm²/V•s in AMI 0.6 μ m process
- ❑ Thus pMOS must be wider to provide same current
 - In this class, assume $\mu_n / \mu_p = 2$



Channel Length Modulation

- ❑ Reverse-biased p-n junctions form a *depletion region*
 - Region between n and p with no carriers
 - Width of depletion L_d region grows with reverse bias
 - $L_{\text{eff}} = L - L_d$
- ❑ Shorter L_{eff} gives **more** current
 - I_{ds} **increases** with V_{ds}
 - Even in saturation



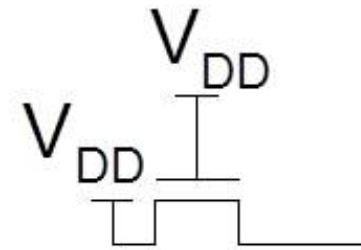
Chan Length Mod I-V

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$

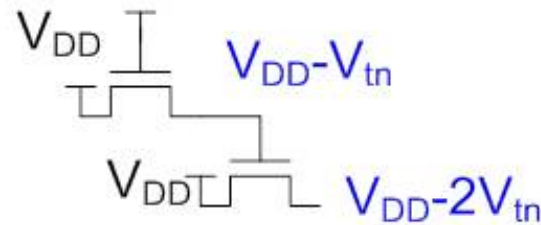
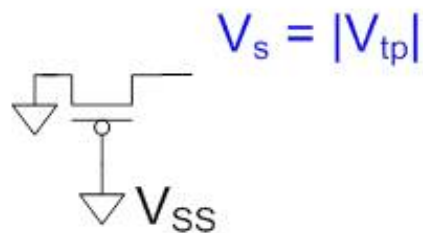
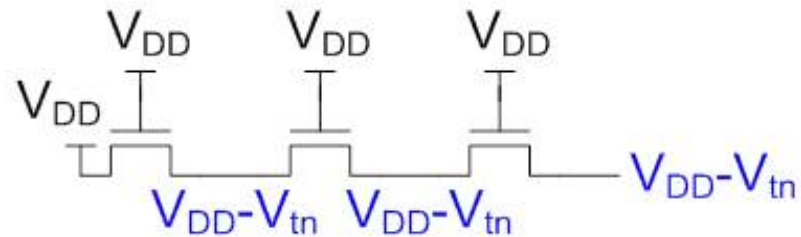
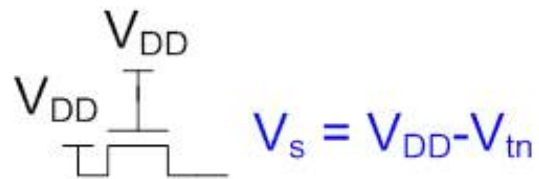
- $\lambda =$ *channel length modulation coefficient*
 - not feature size
 - Empirically fit to I-V characteristics

Pass Transistors

- ❑ We have assumed source is grounded
- ❑ What if source > 0 ?
 - e.g. pass transistor passing V_{DD}
- ❑ $V_g = V_{DD}$
 - If $V_s > V_{DD} - V_t$, $V_{gs} < V_t$
 - Hence transistor would turn itself off
- ❑ nMOS pass transistors pull no higher than $V_{DD} - V_{tn}$
 - Called a degraded “1”
 - Approach degraded value slowly (low I_{ds})
- ❑ pMOS pass transistors pull no lower than V_{tp}
- ❑ Transmission gates are needed to pass both 0 and 1



Pass Transistor Ckts



DC Response

□ DC Response: V_{out} vs. V_{in} for a gate

□ Ex: Inverter

– When $V_{in} = 0$ $\rightarrow V_{out} = V_{DD}$

– When $V_{in} = V_{DD}$ $\rightarrow V_{out} = 0$

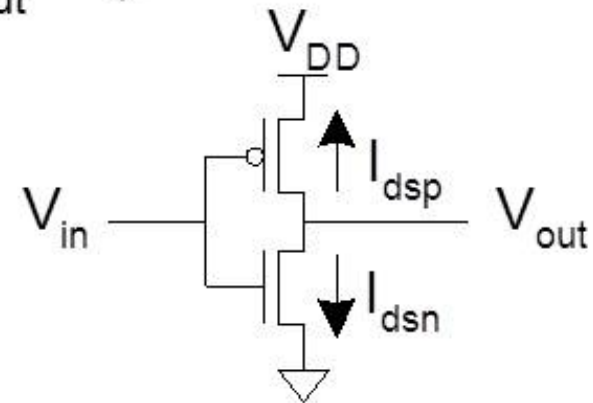
– In between, V_{out} depends on transistor size and current

– By KCL, must settle such that

$$I_{dsn} = |I_{dsp}|$$

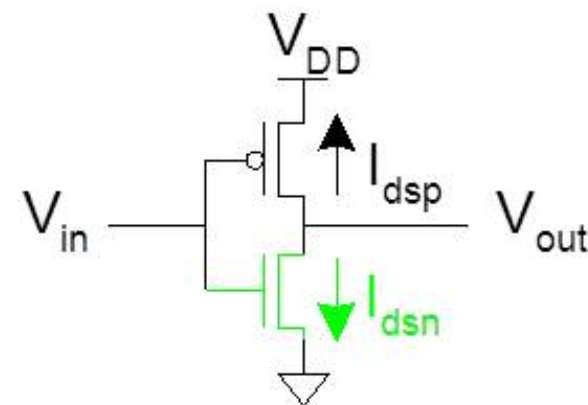
– We could solve equations

– But graphical solution gives more insight



nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$



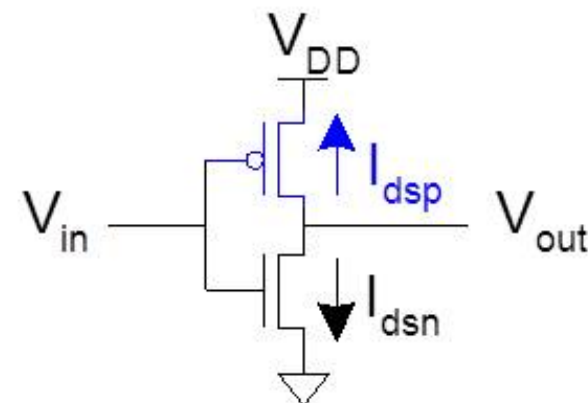
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$$V_{gsp} = V_{in} - V_{DD}$$

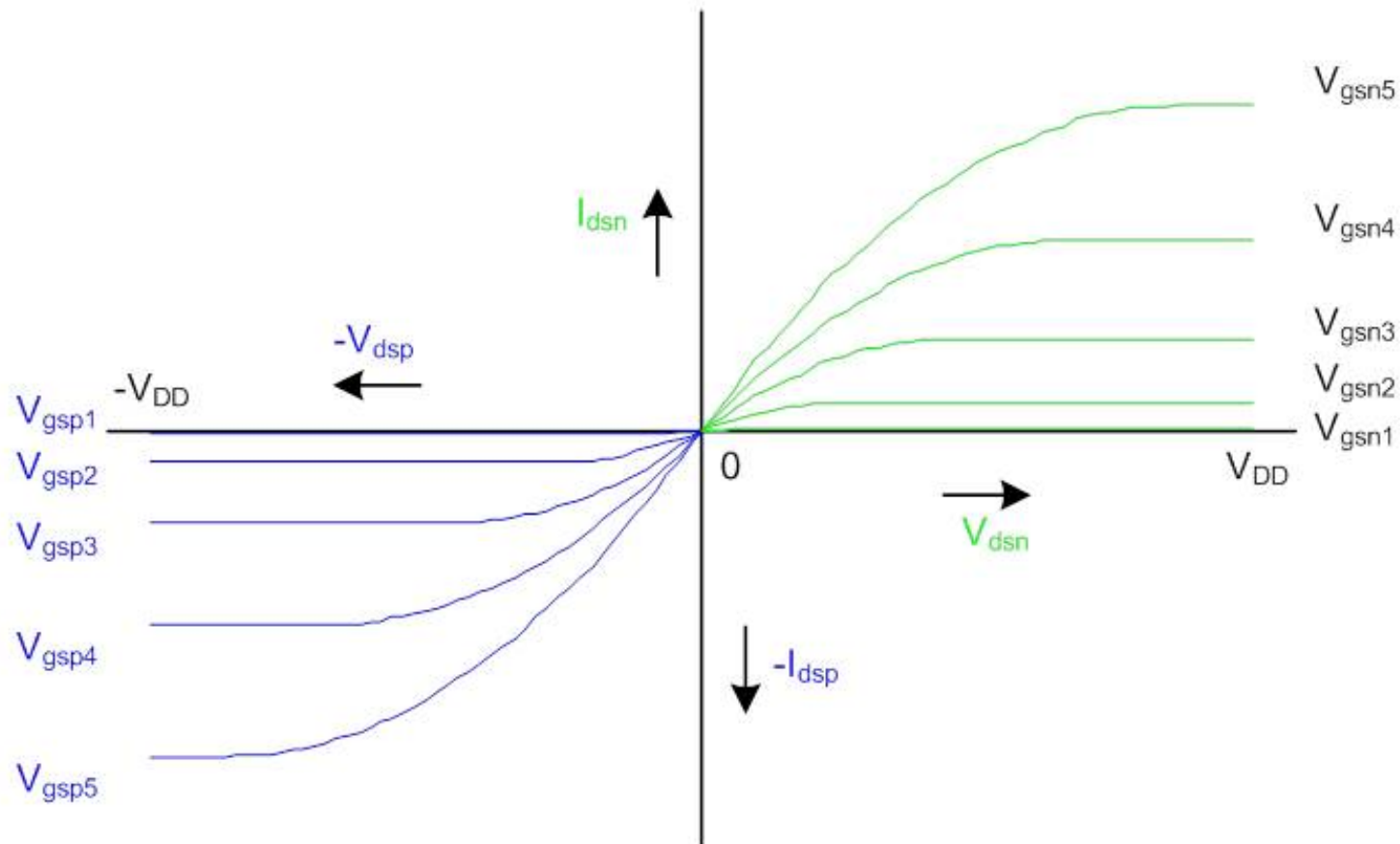
$$V_{tp} < 0$$

$$V_{dsp} = V_{out} - V_{DD}$$

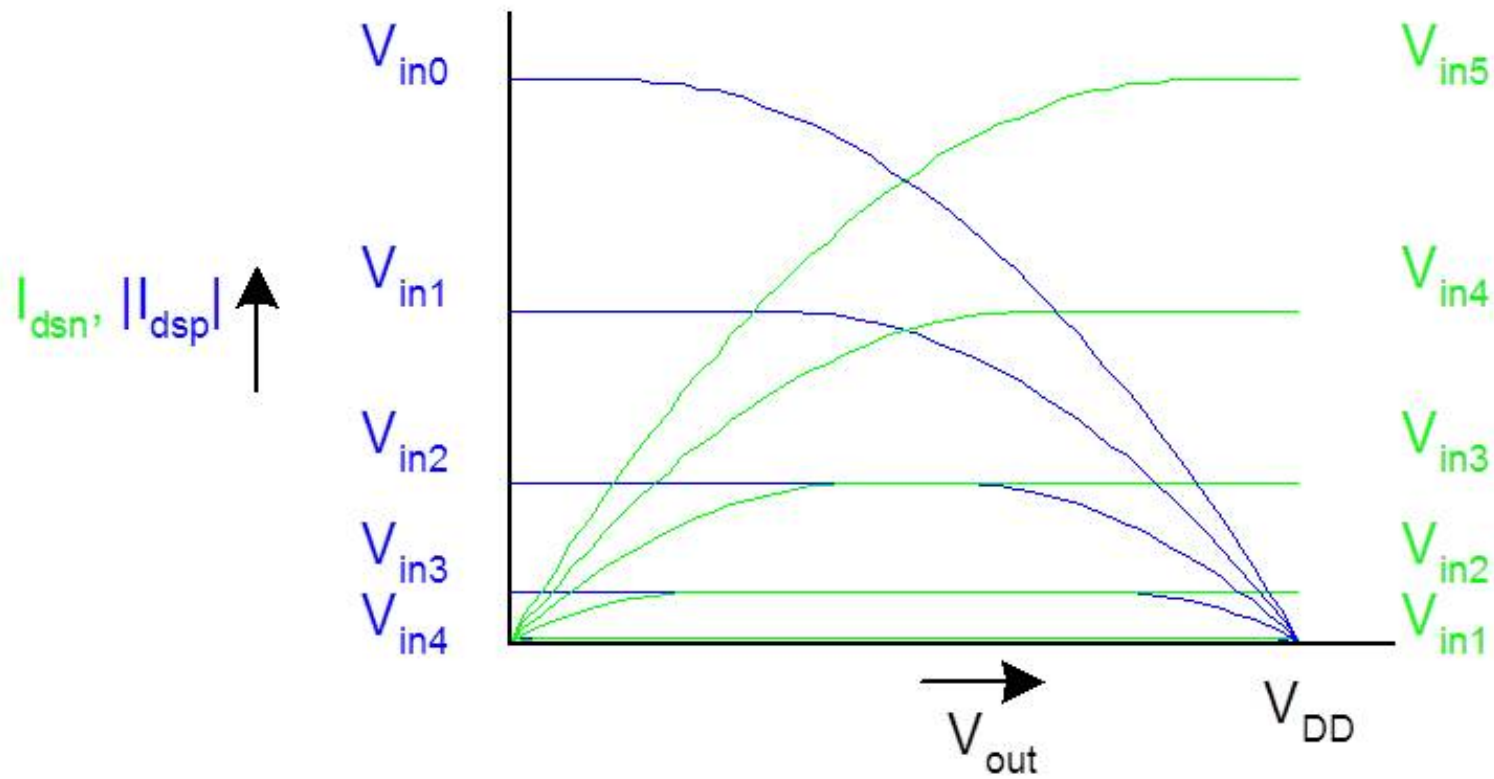


I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

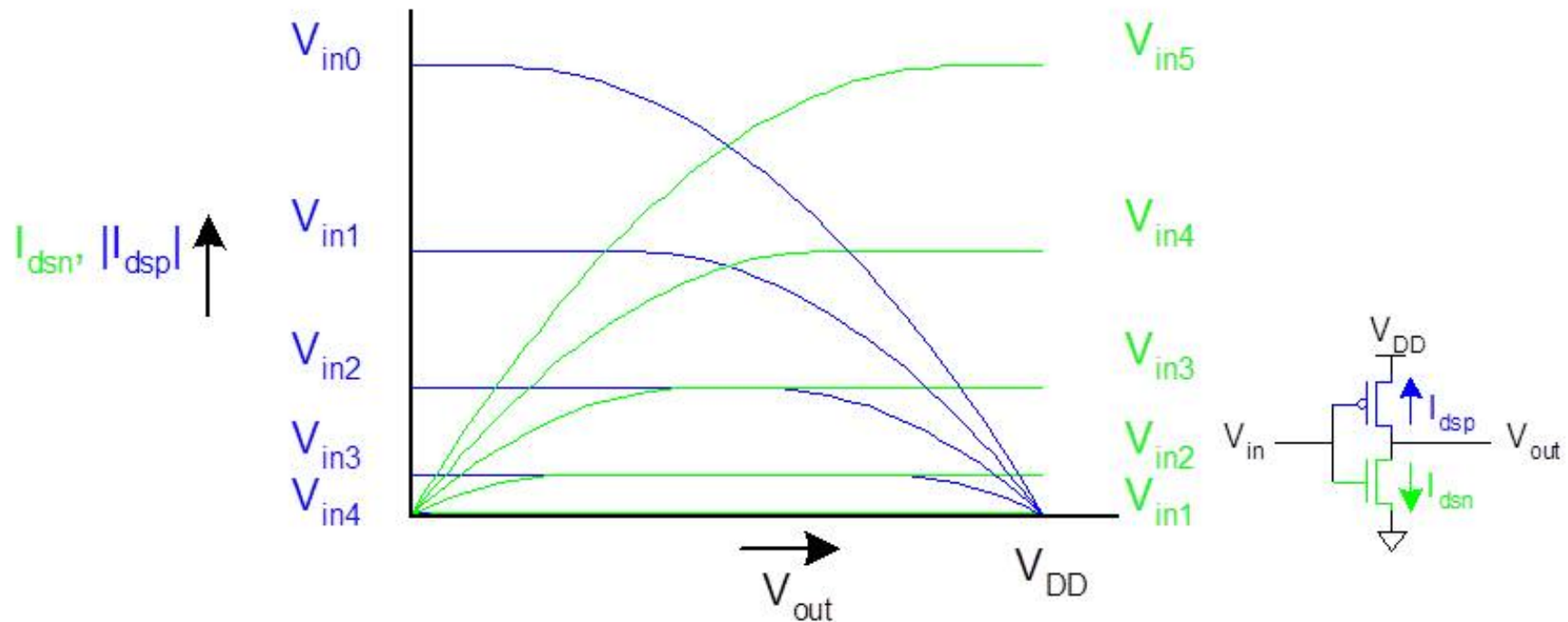


Current vs. V_{out} , V_{in}



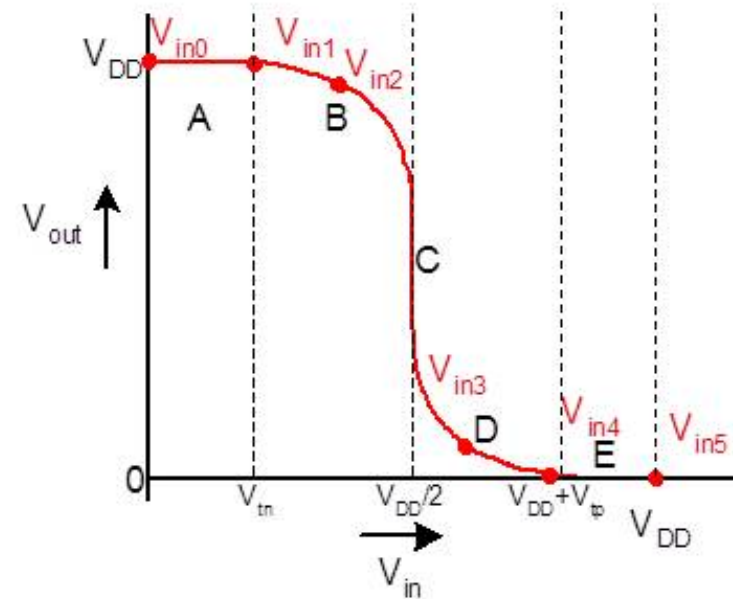
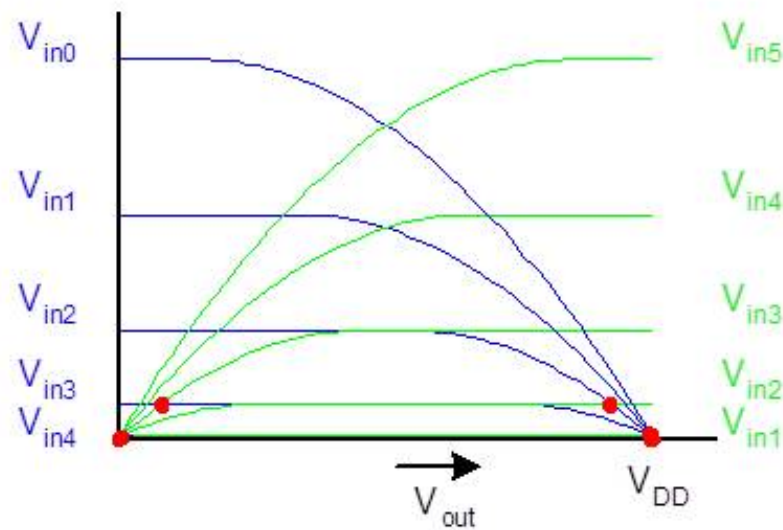
Load Line Analysis

- For a given V_{in} :
 - Plot I_{dsn} , I_{dsp} vs. V_{out}
 - V_{out} must be where |currents| are equal in



DC Transfer Curve

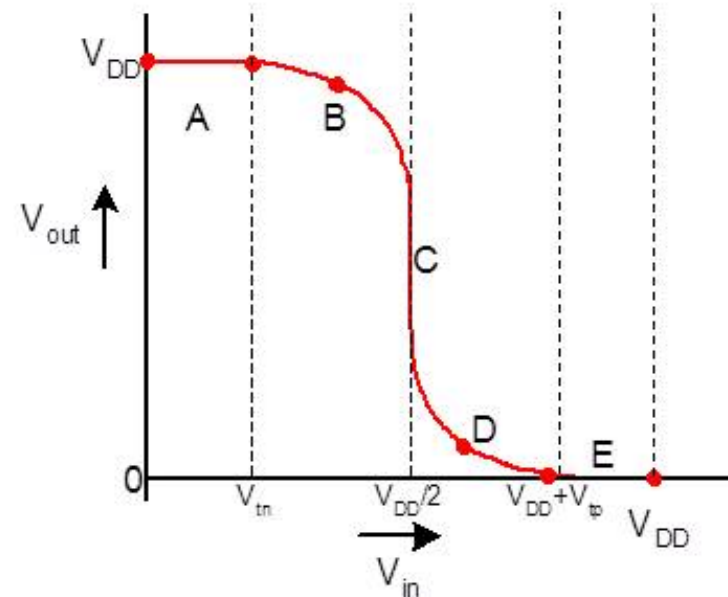
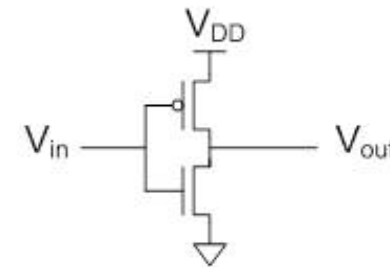
- Transcribe points onto V_{in} vs. V_{out} plot



Operating Regions

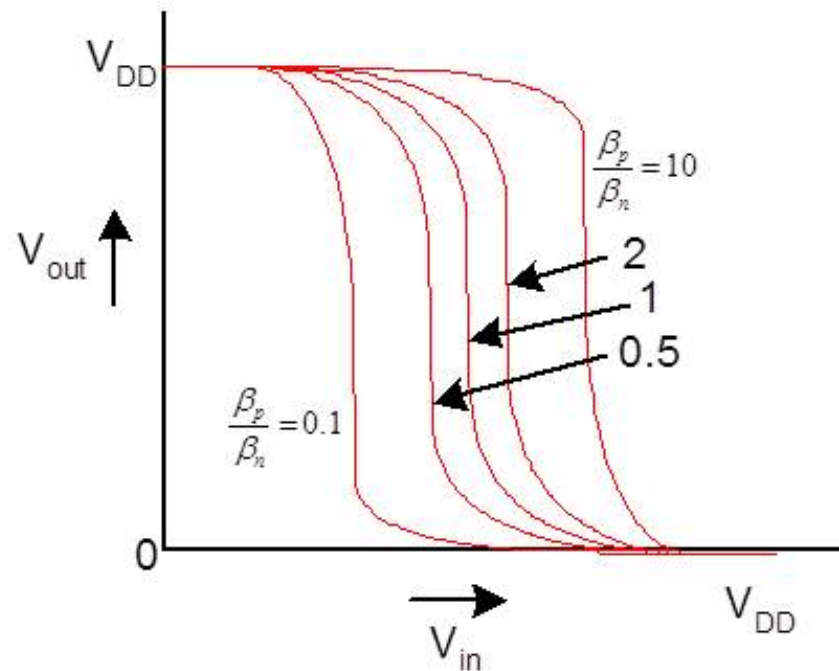
- Revisit transistor operating regions

Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



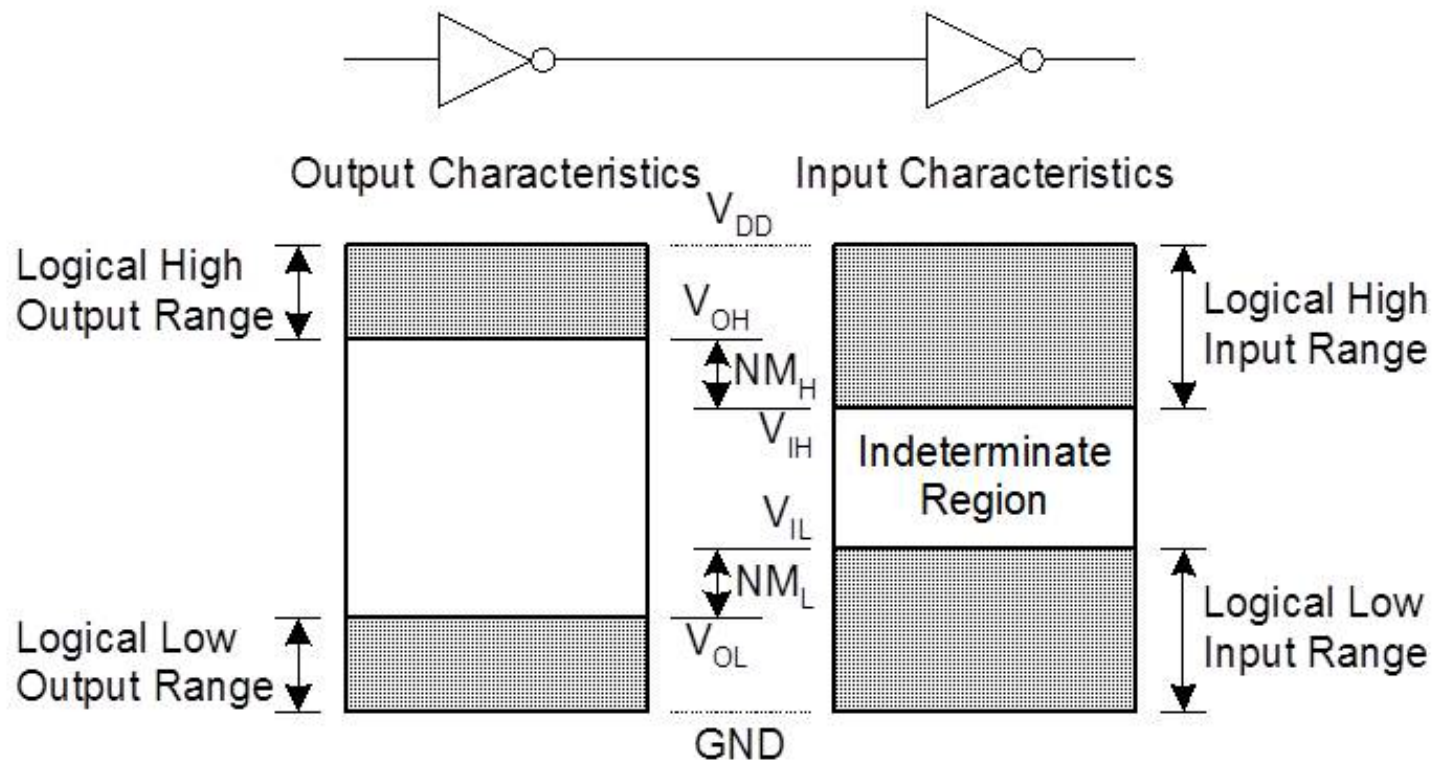
Beta Ratio

- ❑ If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- ❑ Called *skewed gate*
- ❑ Other gates: collapse into equivalent inverter



Noise Margins

- How much noise can a gate input see before it does not recognize the input?



Logic Levels

- ❑ To maximize noise margins, select logic levels at
 - unity gain point of DC transfer characteristic

