UNIT-II

Digital Logic Circuits

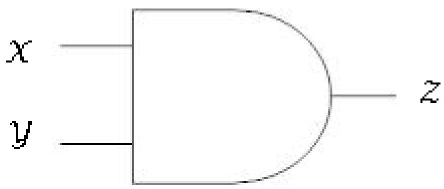
Logic Gates

- A logic gate is an electronic circuit/device which makes the logical decisions.
- To arrive at this decisions, the most common logic gates used are OR, AND, NOT, NAND, and NOR gates.
- The NAND and NOR gates are called universal gates.
- The exclusive-OR gate is another logic gate which can be constructed using AND, OR and NOT gate.
- Logic gates have one or more inputs and only one output. The output is active only for certain input combinations. Logic gates are the building blocks of any digital circuit.
- Logic gates are also called switches. With the advent of integrated circuits, switches have been replaced by TTL (Transistor Transistor Logic) circuits and CMOS circuits.
- Following are the types of gates:
- AND
- OR
- NOT
- NAND
- NOR
- XOR
- XNOR

1. AND Gate

- The AND gate performs logical multiplication, commonly known as AND function.
- The AND gate has two or more inputs and single output.
- The output of AND gate is HIGH only when all its inputs are HIGH (i.e. even if one input is LOW, Output will be LOW).
- If X and Y are two inputs, then output F can be represented mathematically as F = X.Y, where dot (.) denotes the AND.

Logic Symbol :-



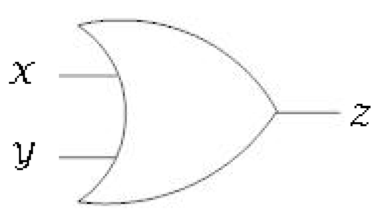
- ***Truth Table :-***

X	Y	F = (X.Y)
0	0	0
0	1	0
1	0	0
1	1	1

2. *OR Gate*

- *The OR gate performs logical addition, commonly known as OR function. The OR gate has two or more inputs and single output.*
- *The output of OR gate is HIGH only when any one of its inputs are HIGH (i.e. even if one input is HIGH, Output will be HIGH).*
- *If X and Y are two inputs, then output F can be represented mathematically as F = X+Y.*
- *Here plus sign (+) denotes the OR operation. Truth table and symbol of the OR gate is shown in the figure below.*

- ***Logic Symbol :-***



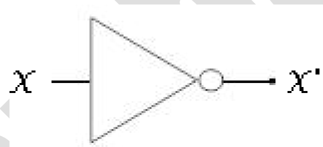
- **Truth Table :-**

X	Y	F = (X+Y)
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT Gate

- The NOT gate performs the basic logical function called inversion or complementation.
- NOT gate is also called inverter.
- The purpose of this gate is to convert one logic level into the opposite logic level. It has one input and one output.
- When a HIGH level is applied to an inverter, a LOW level appears on its output and vice versa.
- If X is the input, then output F can be represented mathematically as F = X', Here apostrophe (') denotes the NOT (inversion) operation.
- There are a couple of other ways to represent inversion, F= !X, here ! represents inversion.
- Truth table and NOT gate symbol is shown in the figure below.

- **Logic Symbol :-**



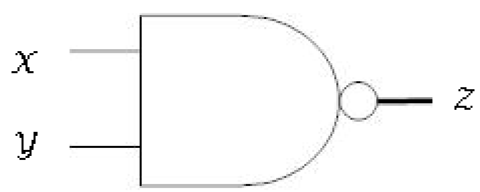
- **Truth Table :-**

X	F = X'
0	1
1	0

4. NAND Gate

- NAND gate is a cascade of AND gate and NOT gate, as shown in the figure below.
- It has two or more inputs and only one output.
- The output of NAND gate is HIGH when any one of its input is LOW (i.e. even if one input is LOW, Output will be HIGH).
- If X and Y are two inputs, then output F can be represented mathematically as F = (X.Y)', here dot (.) denotes the AND operation and (') denotes inversion.
- Truth table and symbol of the N AND gate is shown in the figure below.

Logic Symbol :-



Truth Table :-

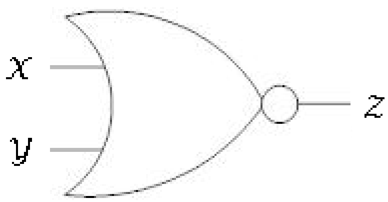
X	Y	F = (X.Y)’
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR Gate

- NOR gate is a cascade of OR gate and NOT gate, as shown in the figure below.
- It has two or more inputs and only one output.
- The output of NOR gate is HIGH when any all its inputs are LOW (i.e. even if one input is HIGH, output will be LOW).
- If X and Y are two inputs, then output F can be represented mathematically as F = (X+Y)'; here plus (+) denotes the OR operation and (') denotes inversion.

- *Truth table and symbol of the NOR gate is shown in the figure below.*

- **Logic Symbol :-**



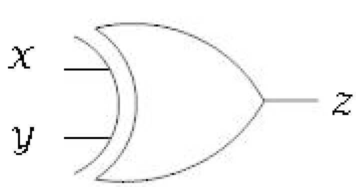
- **Truth Table :-**

X	Y	F = (X.Y)’
0	0	1
0	1	1
1	0	1
1	1	0

6. XOR Gate

- *An Exclusive-OR (XOR) gate is gate with two or three or more inputs and one output.*
- *The output of a two-input XOR gate assumes a HIGH state if one and only one input assumes a HIGH state.*
- *This is equivalent to saying that the output is HIGH if either input X or input Y is HIGH exclusively, and LOW when both are 1 or 0 simultaneously.*
- *If X and Y are two inputs, then output F can be represented mathematically as $F = X \oplus Y$, here $\oplus$ denotes the XOR operation. $X \oplus Y$ and is equivalent to $X.Y' + X'.Y$.*
- *Truth table and symbol of the XOR gate is shown in the figure below.*

- **Logic Symbol :-**



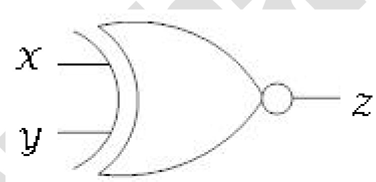
- **Truth Table :-**

X	Y	$F = (X \oplus Y)$
0	0	1
0	1	1
1	0	1
1	1	0

7. XNOR Gate

- The exclusive – NOR gate, abbreviated Ex – NOR, is an Ex – OR fate, followed by an inverter.
- An Exclusive-NOR (XNOR) gate is gate with two or three or more inputs and one output.
- The output of a two-input XNOR gate assumes a HIGH state if all the inputs assumes same state.
- This is equivalent to saying that the output is HIGH if both inputs X and Y is HIGH exclusively or same as input X and input Y is LOW exclusively, and LOW when both are not same.
- If X and Y are two inputs, then output F can be represented mathematically as $F = \overline{x \oplus y}$ and is equivalent to X.Y + X'.Y'.
- Truth table and symbol of the XNOR gate is shown in the figure below.

- **Logic Symbol :-**



- **Truth Table :-**

X	Y	$F = (\overline{x \oplus y})$
0	0	1
0	1	0
1	0	0
1	1	1

SHIFT REGISTERS

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SHIFT REGISTERS

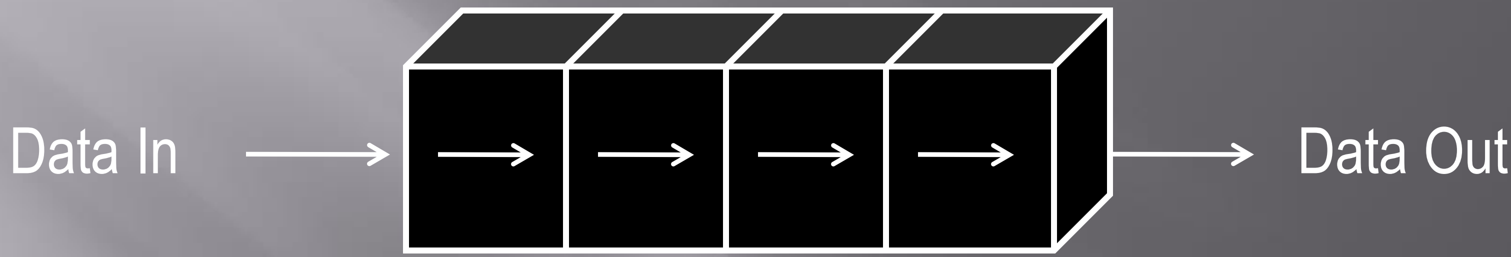
- Shift registers are a type of sequential logic circuit, mainly for storage of digital data.

- A register that is capable of shifting data one bit at a time is called a shift register.

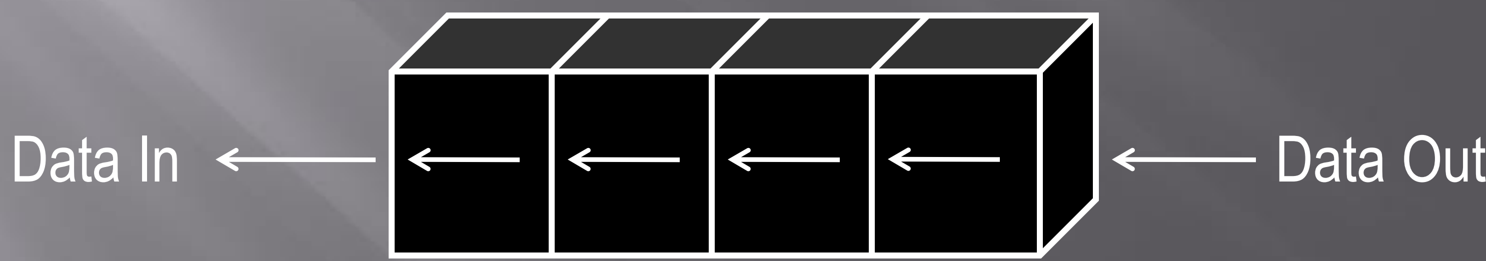
- The logical configuration of a serial shift register consists of a chain of flip-flops connected in cascade, with the output of one flip-flop being connected to the input of its neighbor.

- The operation of the shift register is synchronous; thus each flip-flop is connected to a common clock.

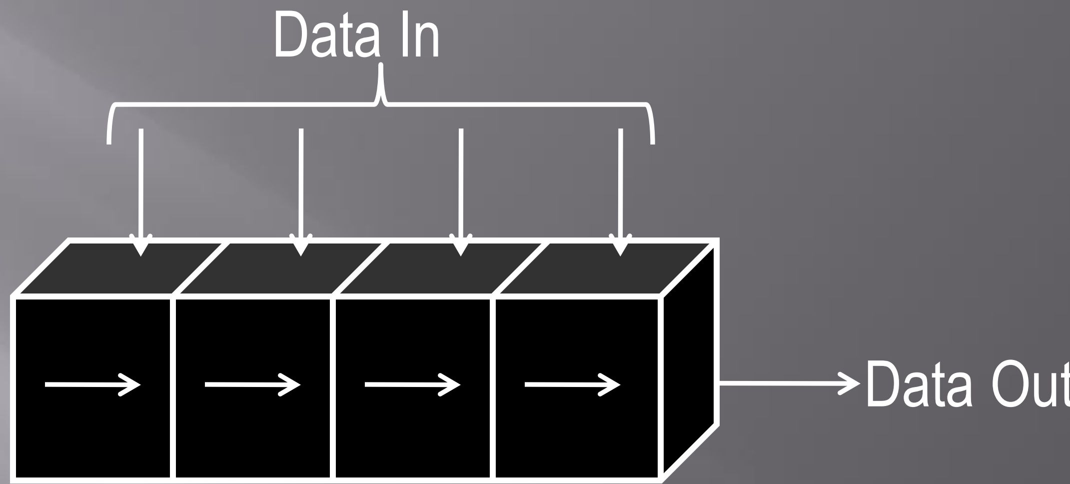
❖ Basic data movement in shift registers [Floyd]



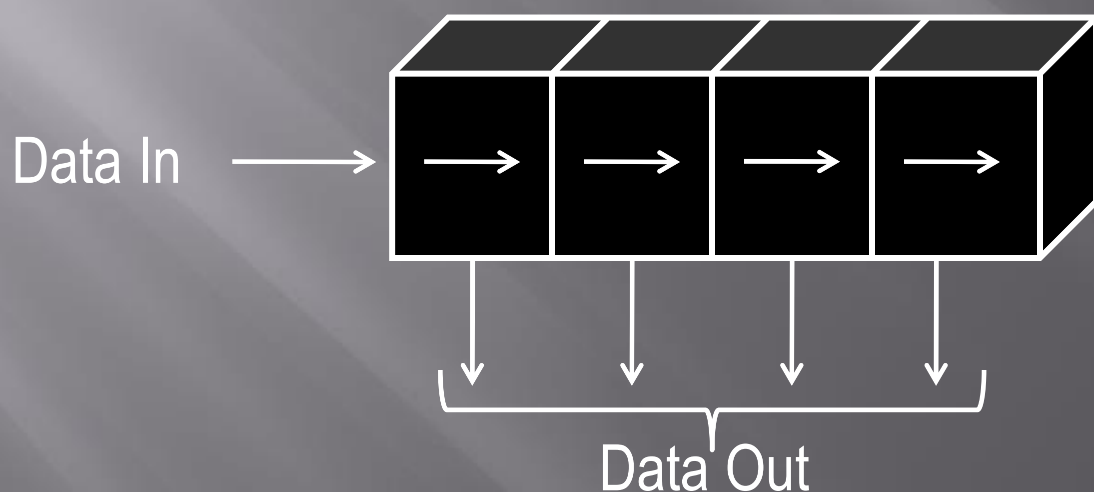
Serial In / Shift Right / Serial Out



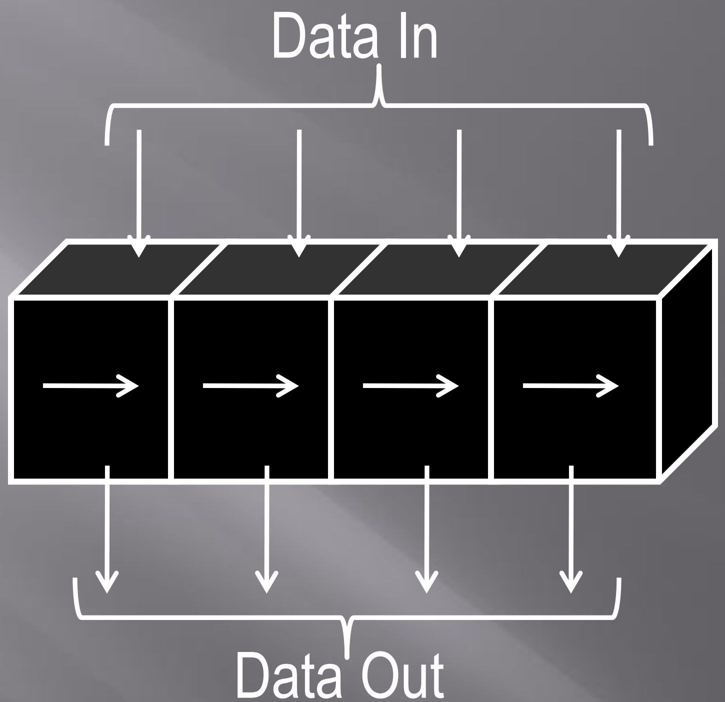
Serial In / Shift Left / Serial Out



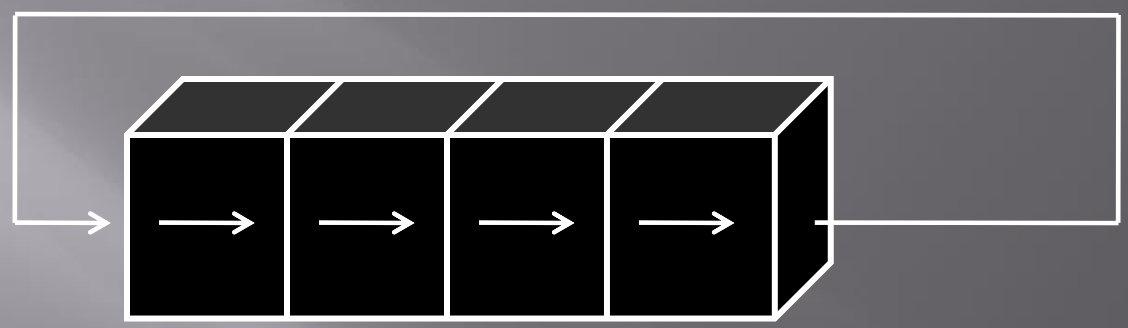
Parallel In / Serial Out



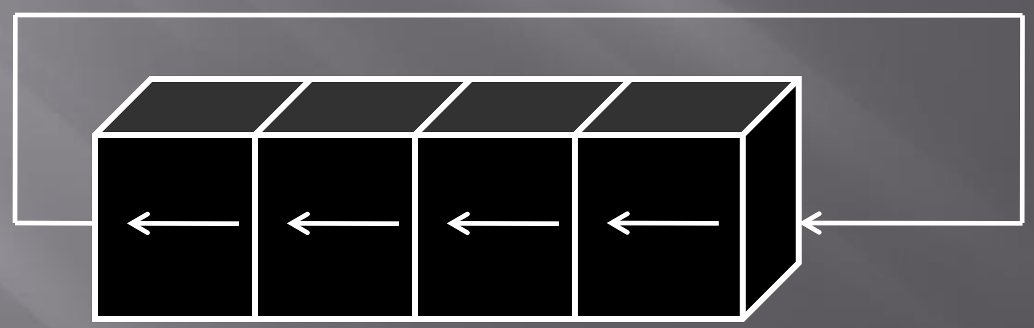
Serial In / Parallel Out



Parallel In / Parallel Out

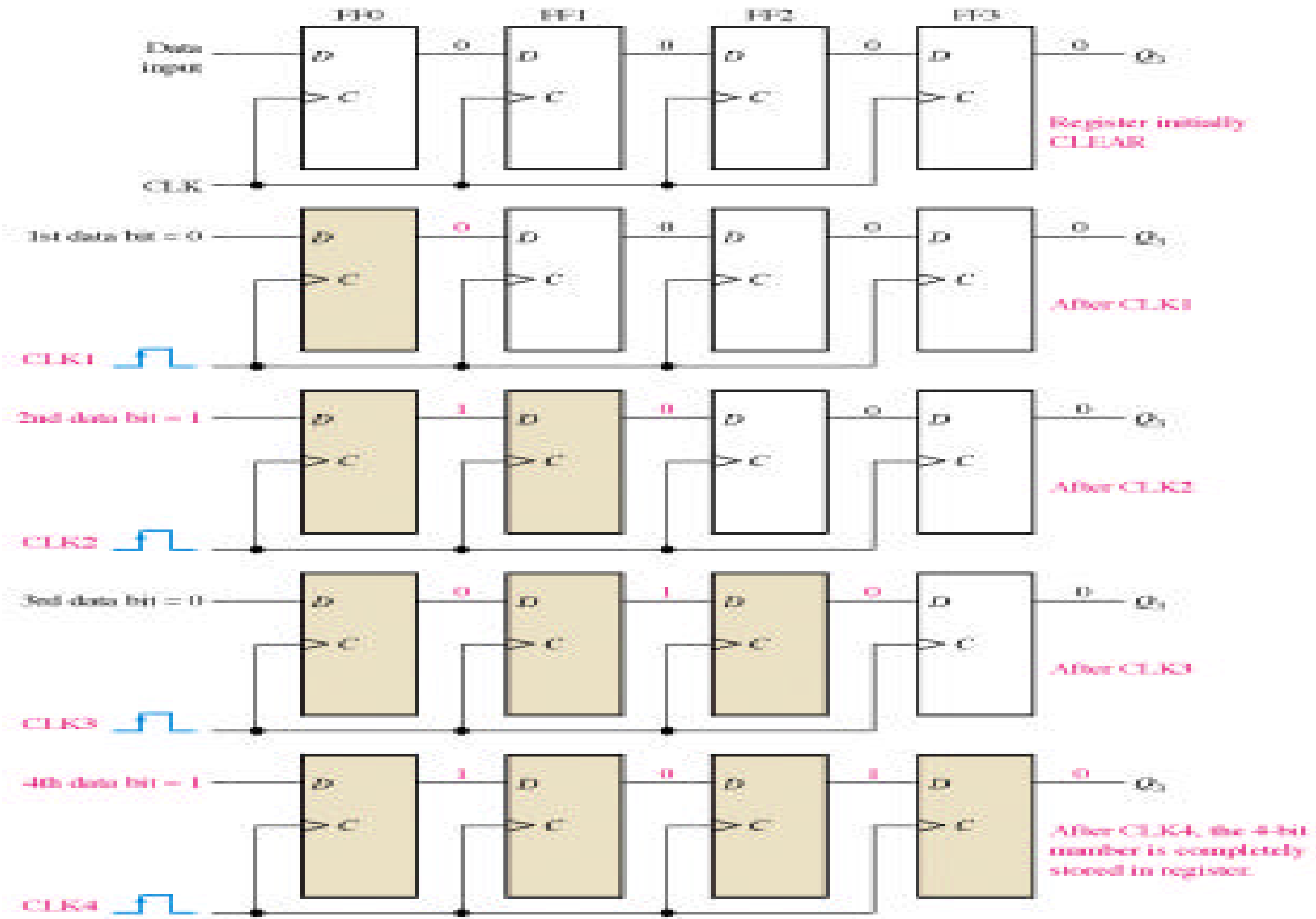


Rotate Right

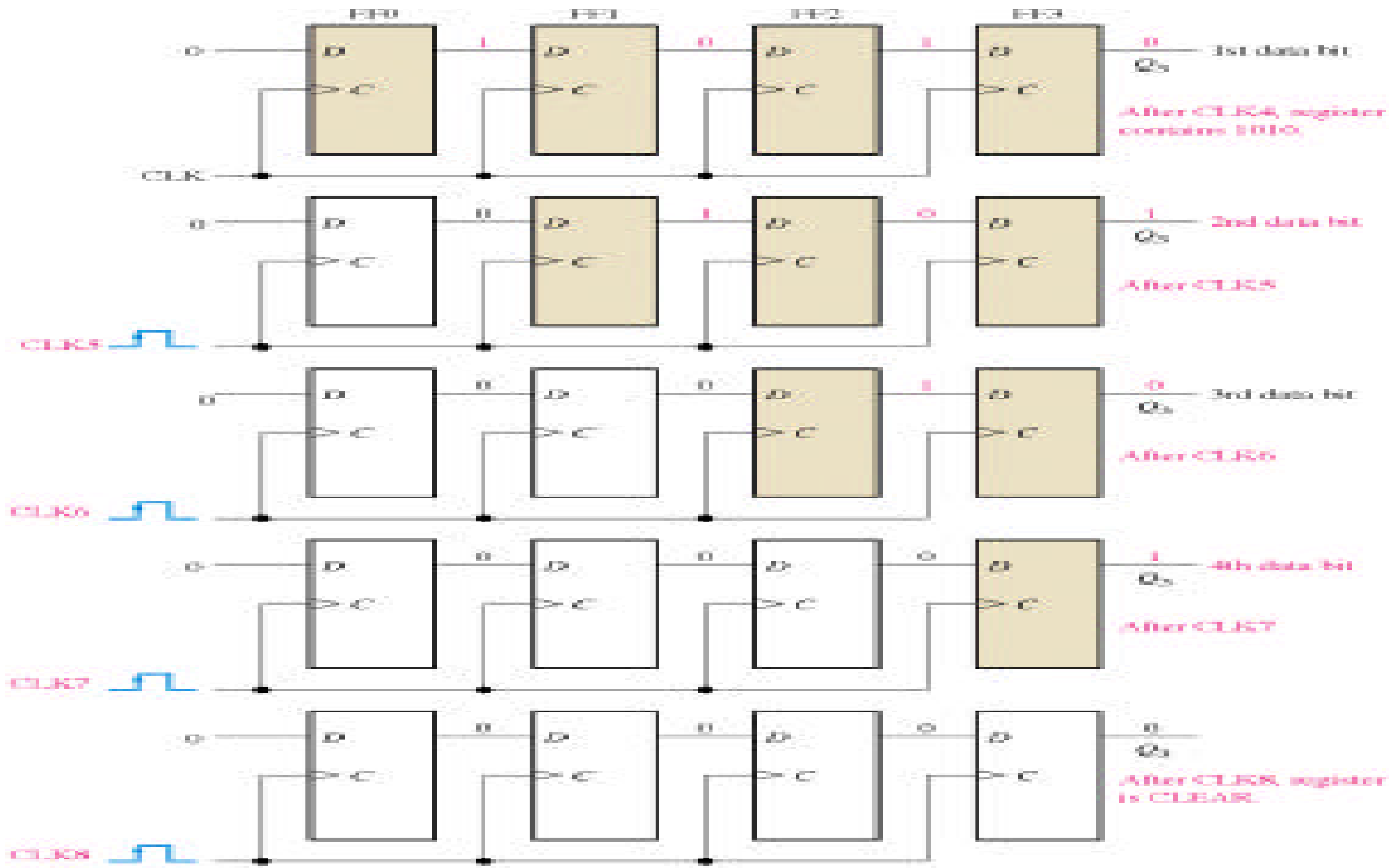


Rotate Left

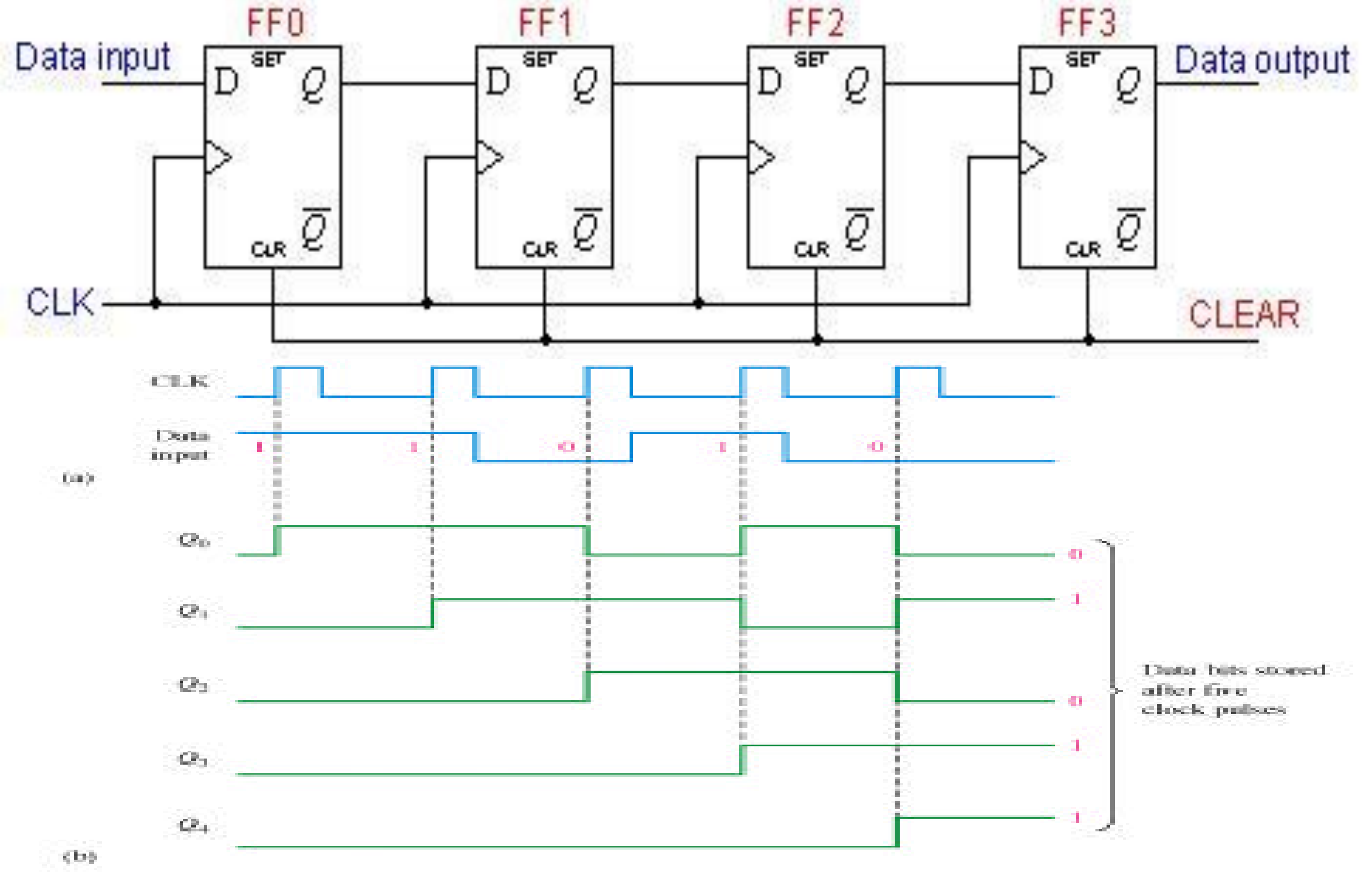
➢Let us illustrate the entry of the four bits 1010 into the register.



- Figure below shows the four bits (1010) being serially shifted out of the register and replaced by all zeros.



❑Figure 1 shows the circuit diagram for a four-bit serial in-serial out shift register implemented using D flip-flops.



UNIT – 2
Asynchronous Counter – Ripple Counter

Counters

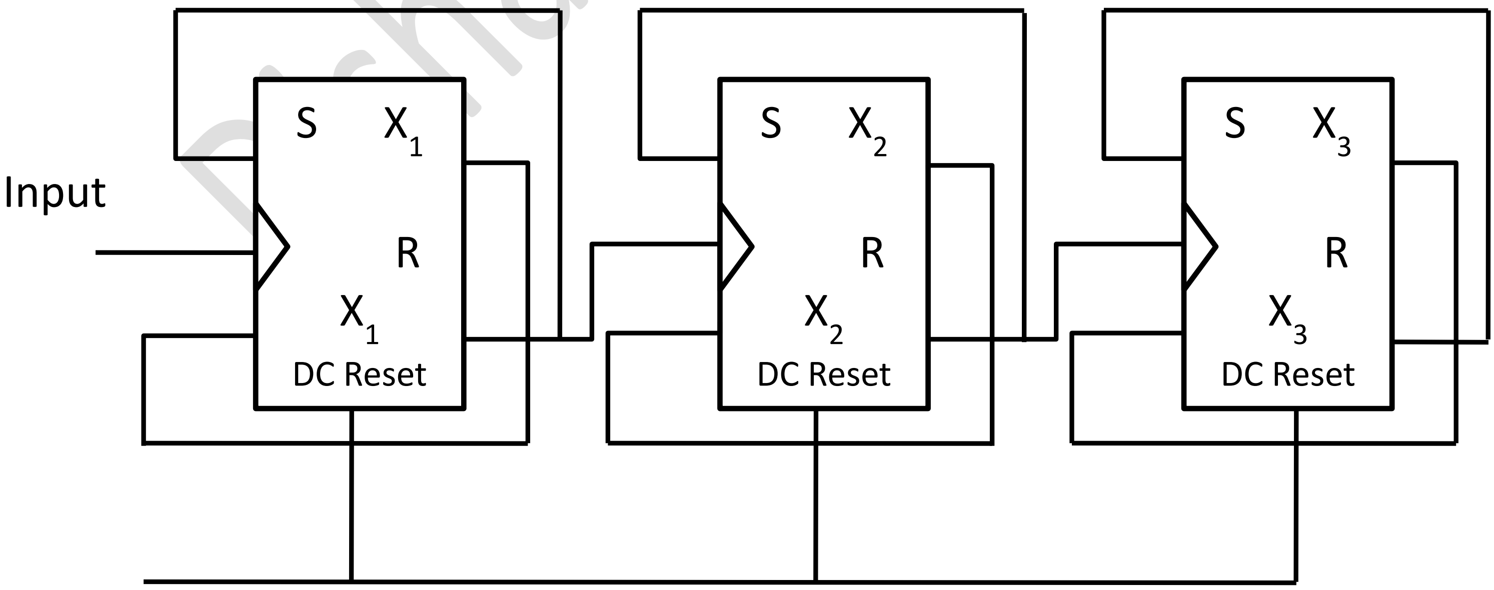
- A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter.
- The input pulses may be clock pulses or they may originated from some external source and may occur at a fixed interval of time or at random.
- A counter that follows the binary number sequence is called a binary counter.
- An n-bit binary counter consists of n flip-flops and can count in binary from 0 through 2^n -1.
- Counters are divided in two categories

  1. Ripple counters

  2. Synchronous counters

Ripple counters

- The flip-flop output transition serves as a source for triggering other flip-flops.
- The C input some or all flip-flops are triggered not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs.
- **Ripple Binary Counter**



Reset Counter